DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

Digital Integrated Circuits - ENCS333

2nd SEMESTER (2015-2016)

Dr. Khader Mohammad

Lecture #6

Introduction

Layout of an Inverter and basic gates

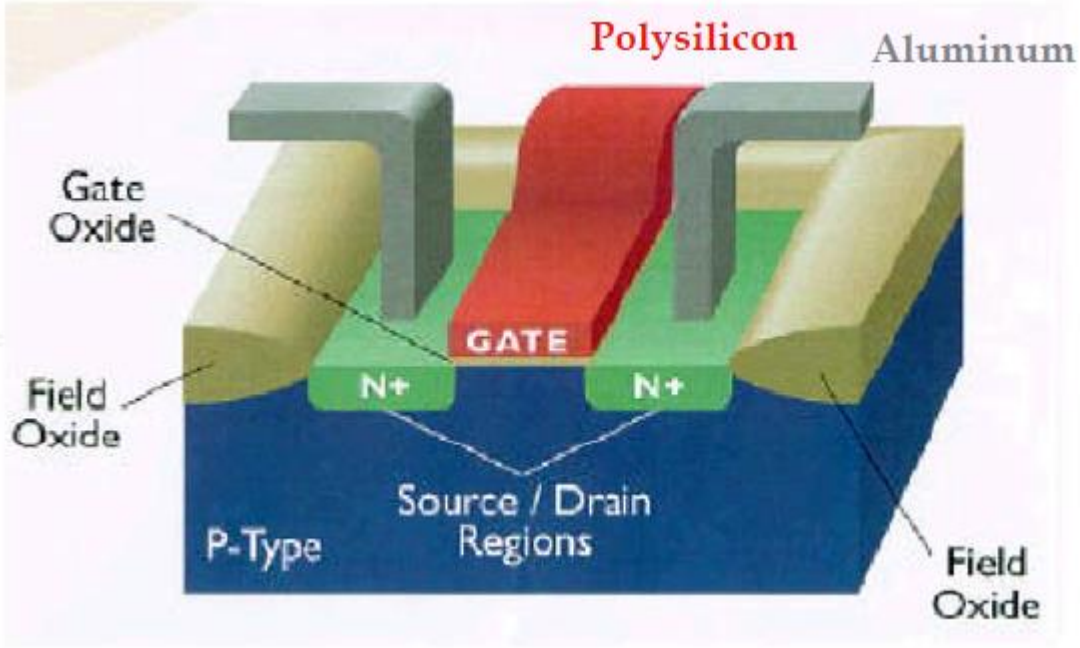
Digital Integrated Circuits

	Course topics and Schedule
	Subject
1	Introduction to Digital Integrated Circuits Design
2	Semiconductor material: pn-junction, NMOS, PMOS
3	IC Manufacturing and Design Metrics CMOS
4	Transistor Devices and Logic Design The CMOS inverter
5	Combinational logic structures
7	Sequential logic gates; Latches and Flip-Flops
6	Layout of an Inverter and basic gates
8	Parasitic Capacitance Estimation
9	Device modeling parameterization from I-V curves.
	Short Test
10	Arithmetic building blocks
11	Interconnect: R, L and C - Wire modeling
12	Timing
	Power dissipation;
13	SPICE Simulation Techniques (Project)
14	Memories and array structures
	Midterm
15	Clock Distribution
16	Supply and Threshold Voltage Scaling
17	Reliability and IC qualification process
18	Advanced Voltage Scaling Techniques
19	Power Reduction Through Switching Activity Reduction
20	CAD tools and algorithms
21	Final & Project discussion

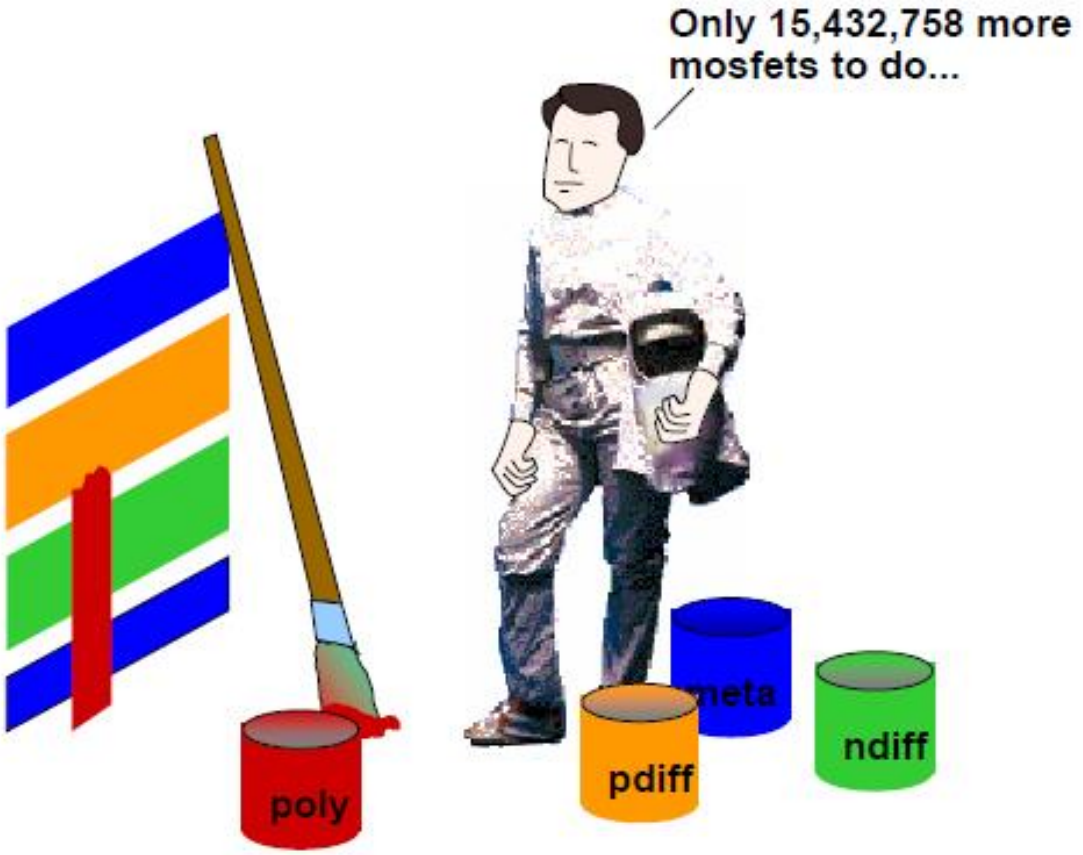
DIGITAL GATES
Fundamental Parameters

- Functionality
- Reliability, Robustness
- Area
- Performance
  - Speed (delay)
  - Power Consumption
  - Energy

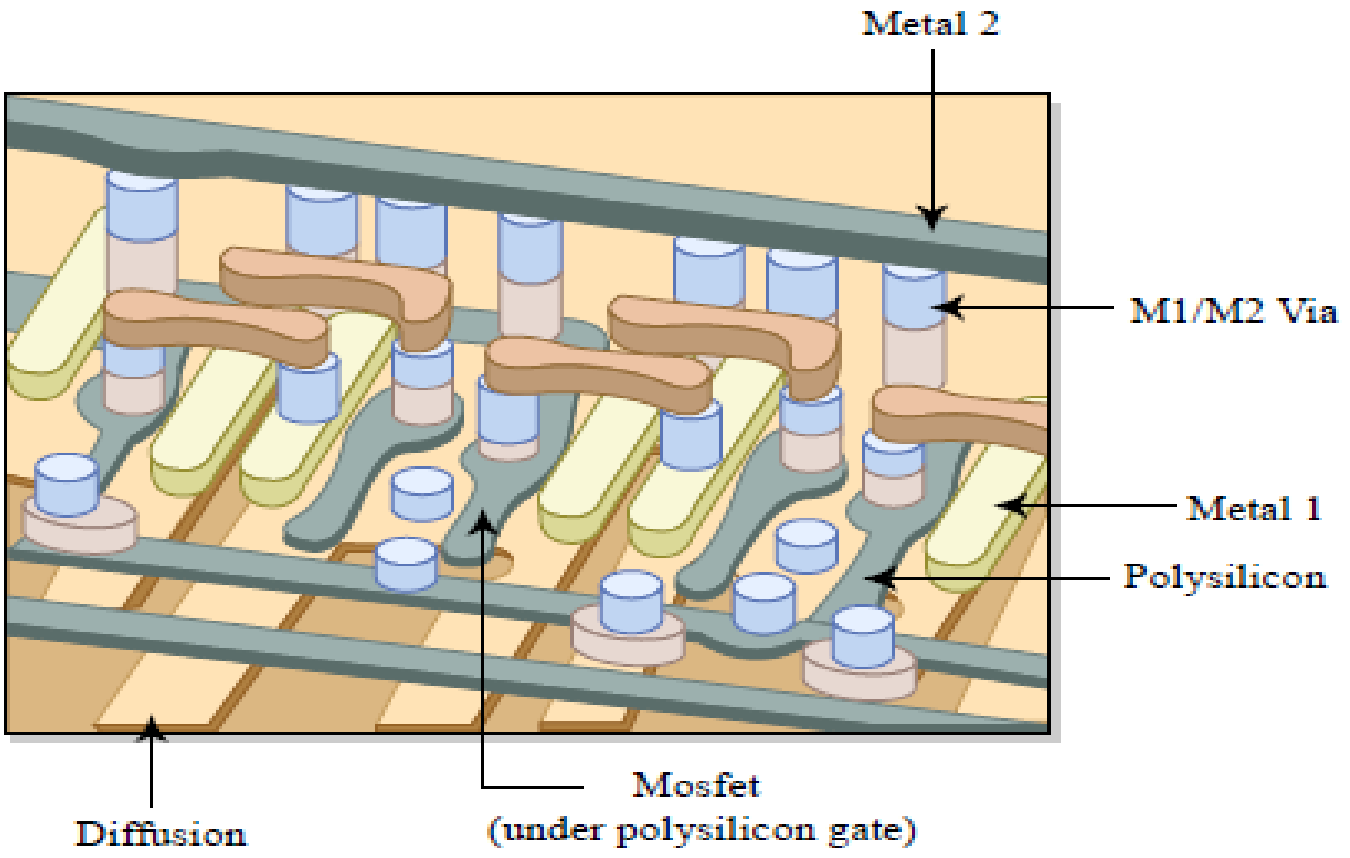
Layout

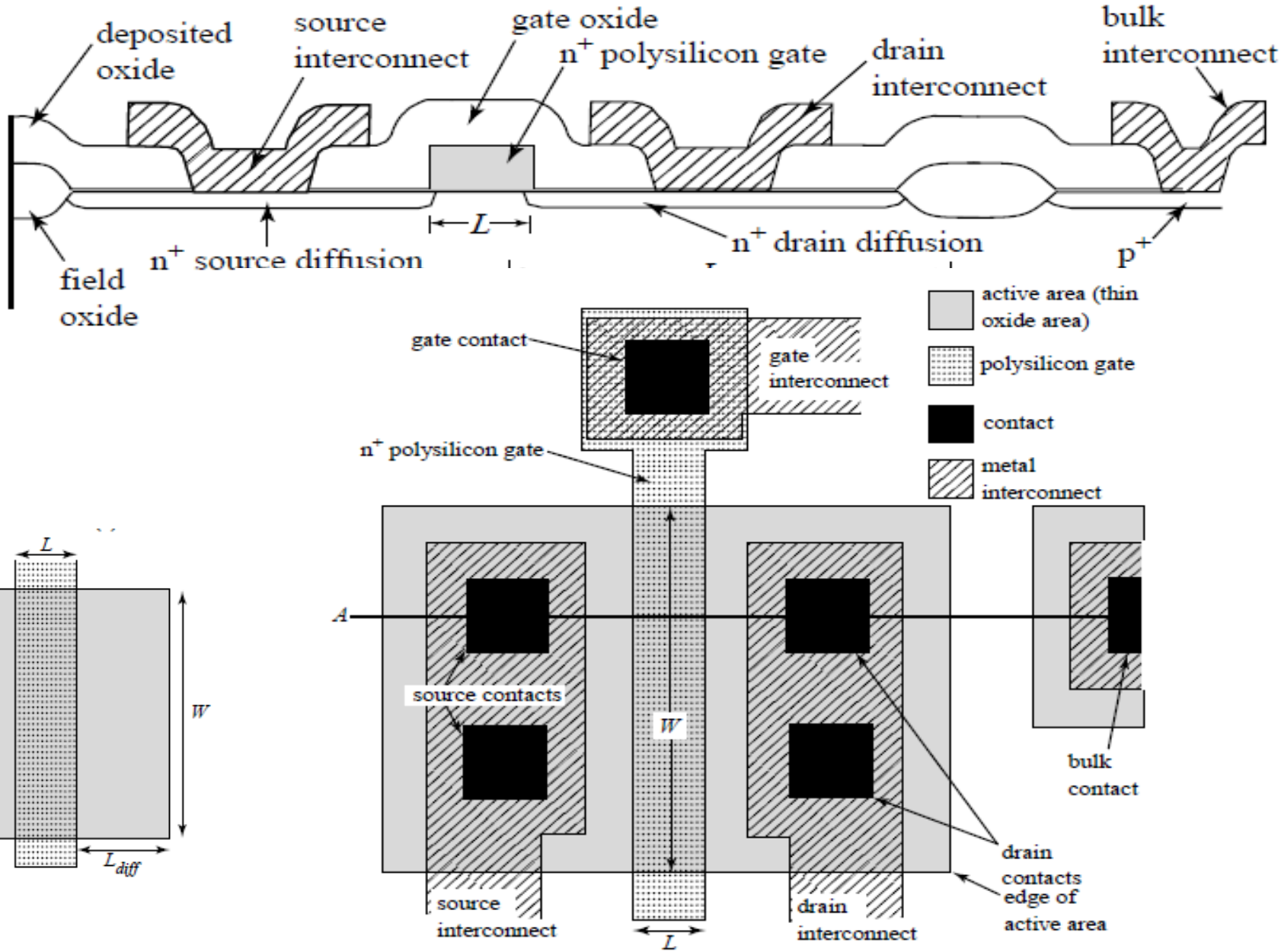

Polysilicon
Aluminum
Gate
Oxide
GATE
N+
N+
Field
Oxide
Source / Drain
Regions
P-Type
Field
Oxide

Layout



Real silicon

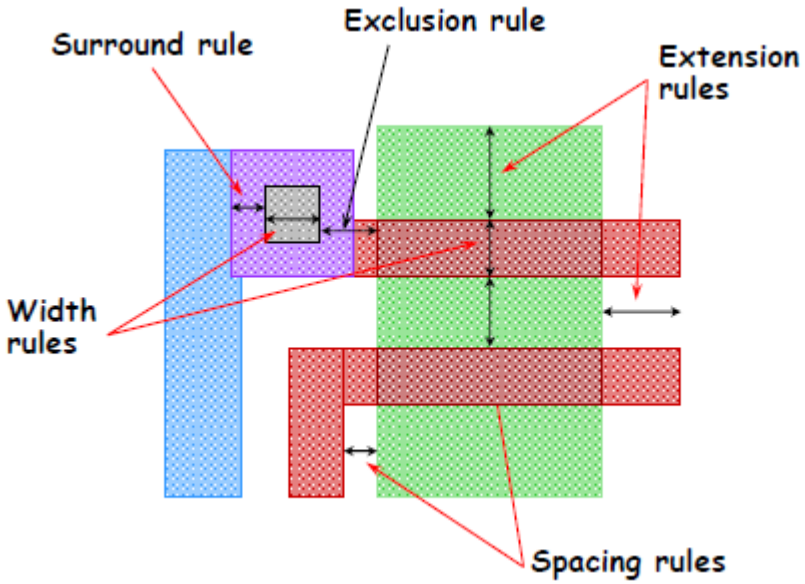



deposited oxide
source interconnect
gate oxide
n+ polysilicon gate
drain interconnect
bulk interconnect
field oxide
n+ source diffusion
L
n+ drain diffusion
p+
active area (thin oxide area)
polysilicon gate
contact
metal interconnect
gate contact
gate interconnect
n+ polysilicon gate
A
source contacts
W
bulk contact
drain contacts
edge of active area
source interconnect
drain interconnect
L
L
W
Ldiff

Process (μ)		0.25	0.18	0.13	0.10	0.07	0.05
V_{DD} (V)		2	1.8	1.5	1.2	0.9	0.7
L_{eff} (nm)		160	100	70	50	35	25
t_{ox} (Å)		50	45	30	25	20	15
Levels		6	6	7	8	9	9
Poly	H (μ)	0.2	0.15	0.13	0.1	0.07	0.07
	W (μ)	0.25	0.18	0.13	0.1	0.07	0.05
	space (μ)	0.25	0.18	0.13	0.1	0.07	0.05
	sheet ρ (Ω/□)	4	5.3	6.2	8	11.4	11.4
M1–2	H (μ)	0.5	0.46	0.34	0.26	0.2	0.14
	W (μ)	0.30	0.23	0.17	0.13	0.1	0.07
	space (μ)	0.30	0.23	0.17	0.13	0.1	0.07
	sheet ρ (Ω/□)	0.044	0.048	0.065	0.085	0.11	0.16
	t_{ins} (nm)	650	500	360	320	270	210
M3–4	H (μ)	0.9	0.8	0.7	0.55	0.4	0.28
	W (μ)	0.6	0.5	0.4	0.3	0.2	0.14
	space (μ)	0.6	0.5	0.4	0.3	0.2	0.14
	sheet ρ (Ω/□)	0.024	0.028	0.031	0.04	0.055	0.079
	t_{ins} (nm)	900	800	700	600	500	400
M5–6	H (μ)	2.5	2.5	1.5	1.2	1.0	0.8
	W (μ)	2.0	2.0	1.0	1.0	0.6	0.5
	space (μ)	2.0	2.0	1.0	1.0	0.6	0.5
	sheet ρ (Ω/□)	0.009	0.009	0.015	0.018	0.022	0.028
	t_{ins} (nm)	1400	1400	900	800	700	600
M7–8	H (μ)	–	–	2.5	2.5	1.5	1.4
	W (μ)	–	–	2.0	2.0	1.0	0.9
	space (μ)	–	–	2.0	2.0	1.0	0.9
	sheet ρ (Ω/□)	–	–	0.009	0.009	0.015	0.016
	t_{ins} (nm)	–	–	1400	1400	900	800
M9	H (μ)	–	–	–	–	2.5	2.5
	W (μ)	–	–	–	–	2.0	2.0
	space (μ)	–	–	–	–	2.0	2.0
	sheet ρ (Ω/□)	–	–	–	–	0.009	0.009
	t_{ins} (nm)	–	–	–	–	1400	1400
Via (M1–M2)	size (μ)	0.55	0.26	0.2	0.16	0.12	0.09
	R (Ω)	0.95	1.32	1.61	2.23	3.35	4.63
κ		3.3	2.7	2.3	2	1.8	1.5

Design Rules

- Design rules are an abstraction of the fabrication process that specify various geometric constraints on how different masks can be drawn.
- Design rules can be absolute measurements (e.g. in nm) or scaled to an abstract unit, the lambda. Lambda-based designs are scaled to the appropriate absolute units depending on the manufacturing process finally used.



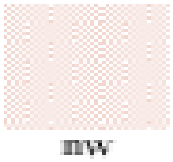
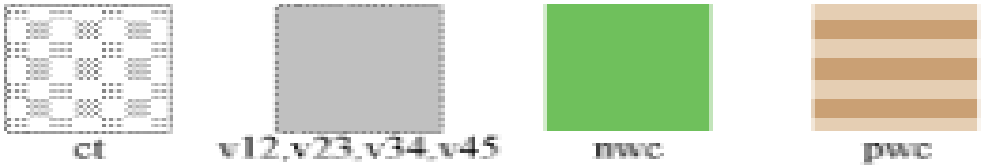
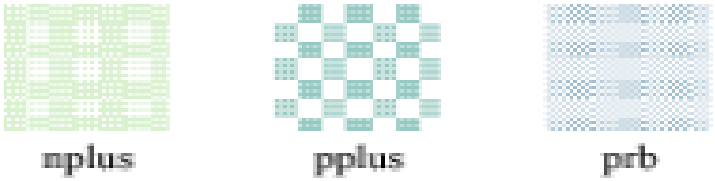
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

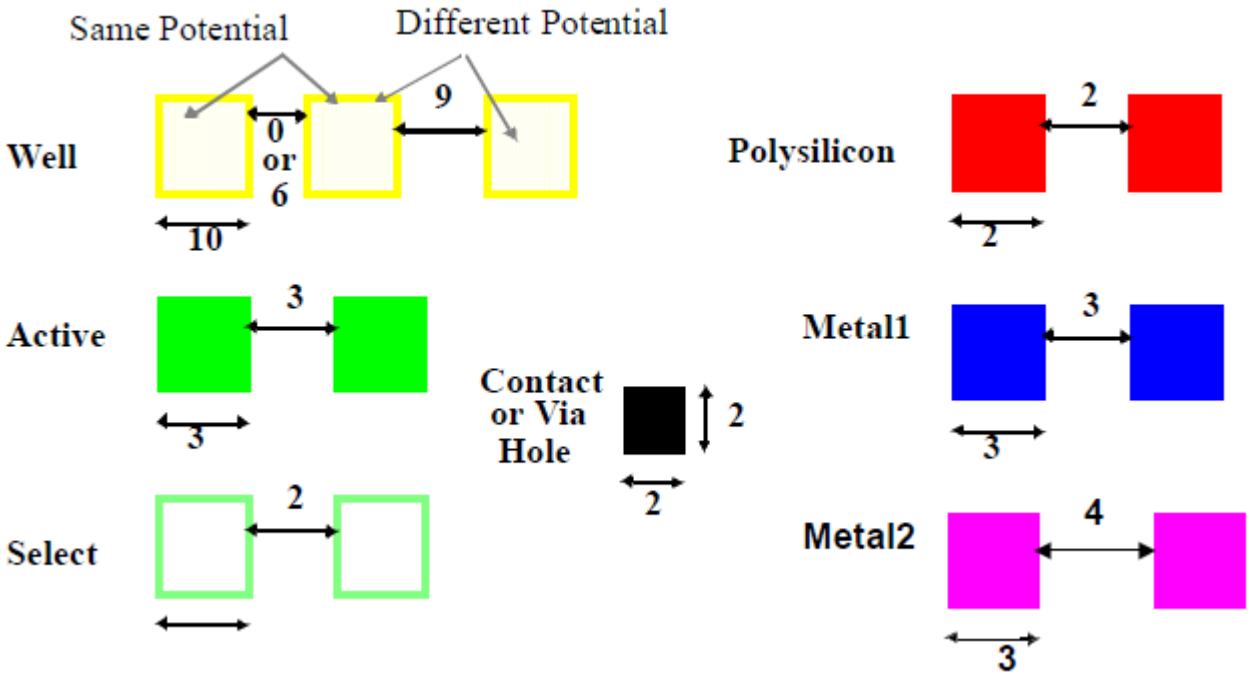
CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

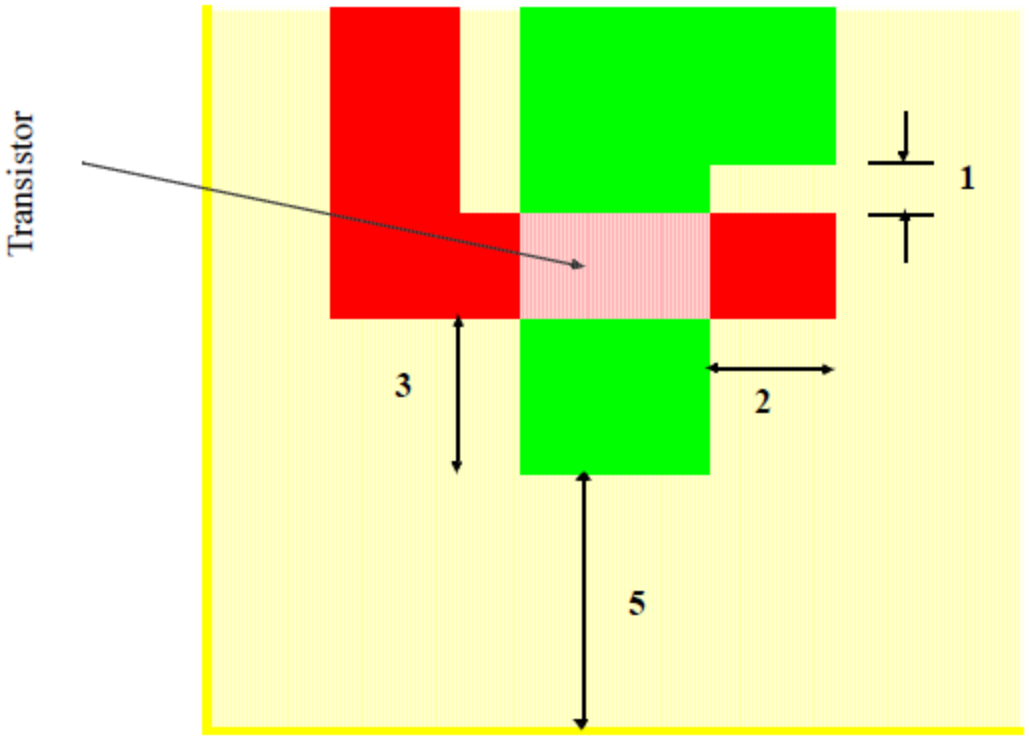
Layers in 0.25 µm CMOS process

Layer Description	Representation
metal	
well	
polysilicon	
contacts & vias	
active area and FETs	
select	

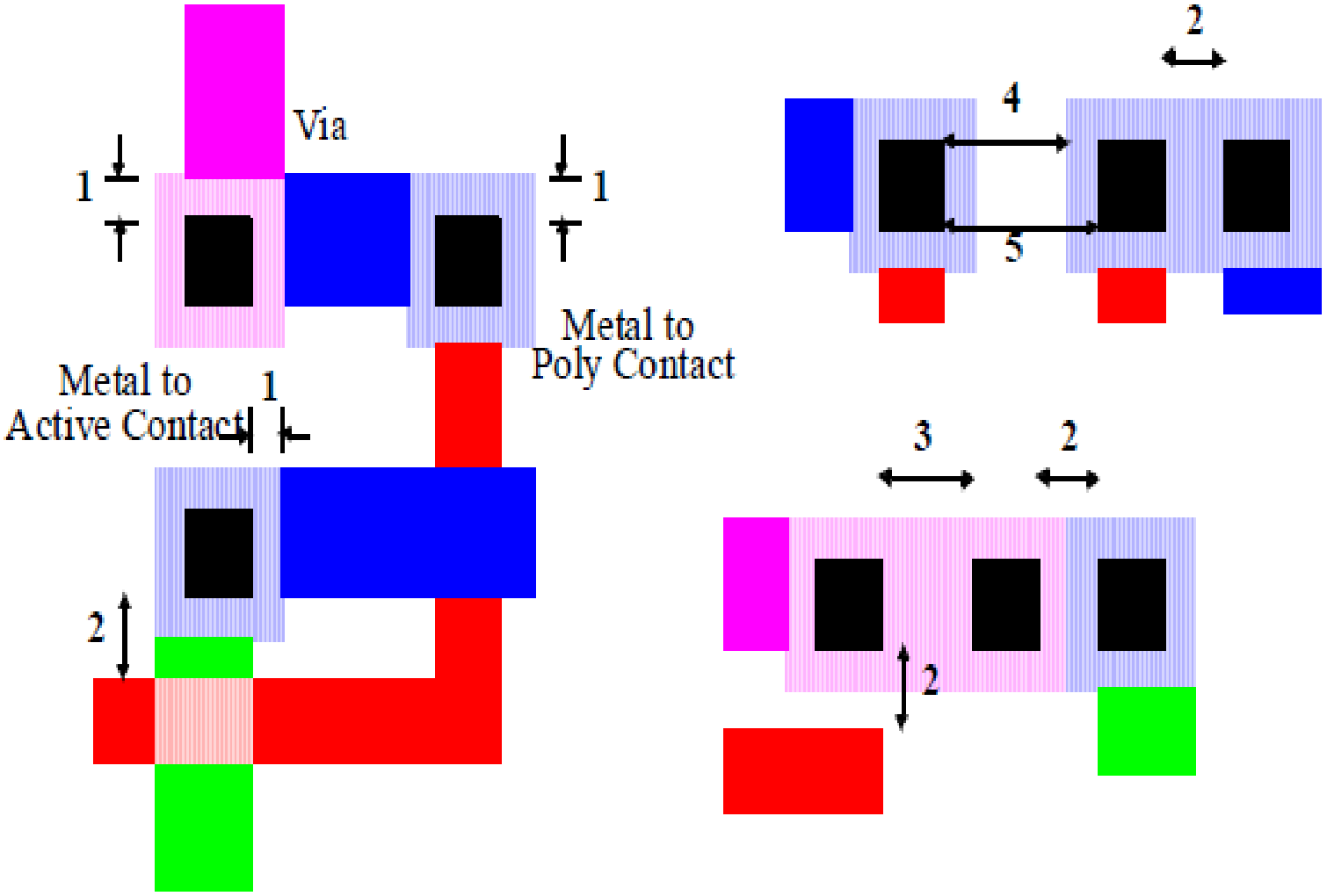
Intra-Layer Design Rules



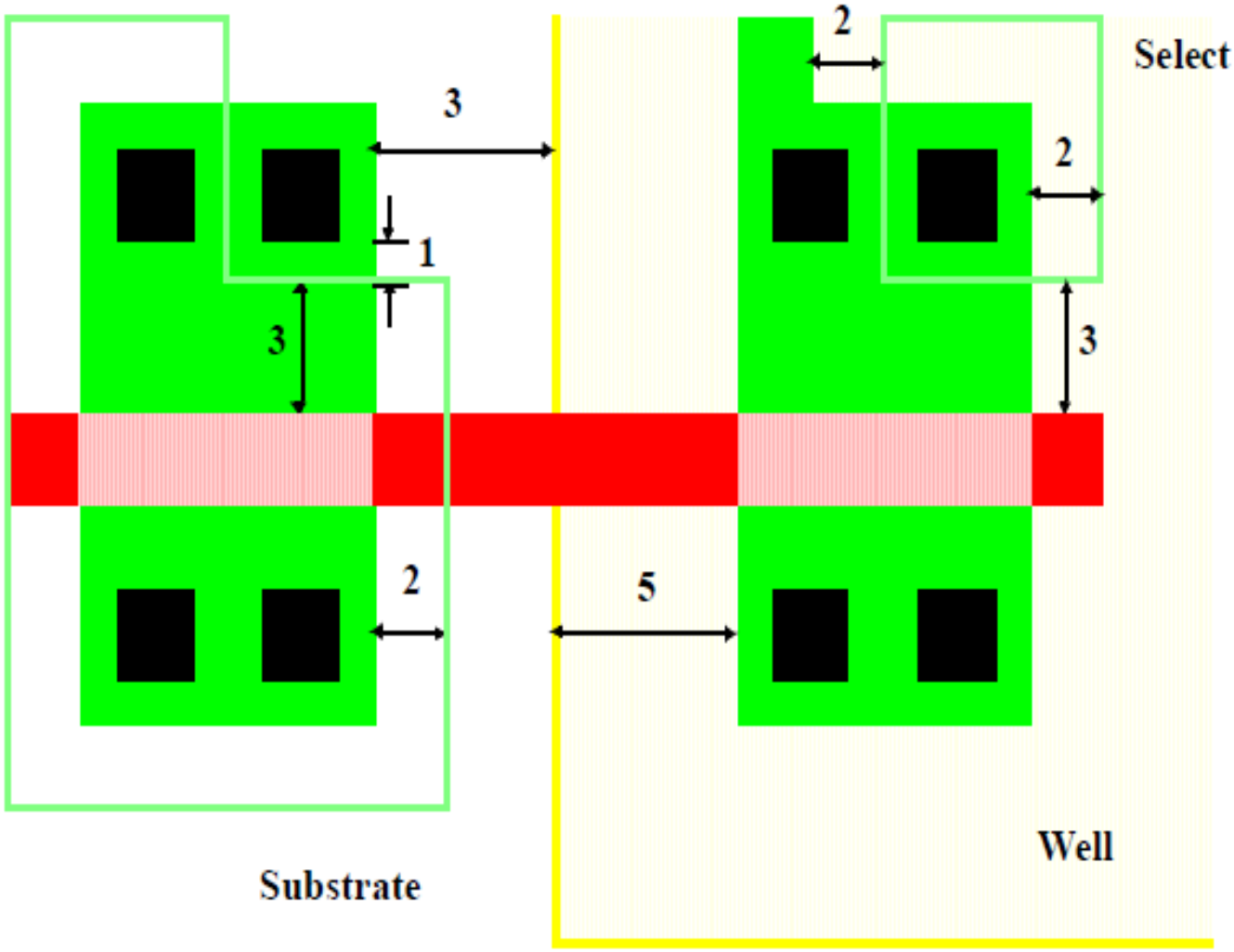
Transistor Layout



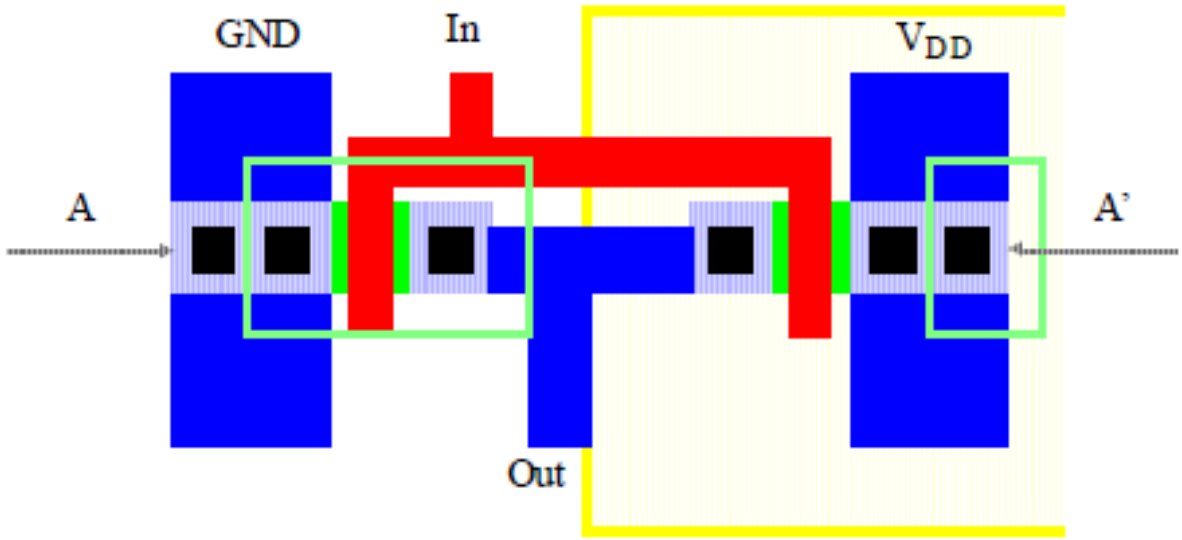
Vias and Contacts



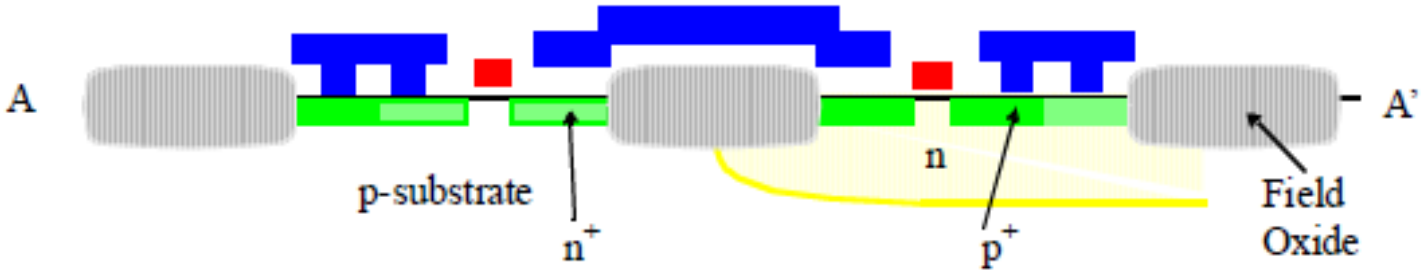
Select Layer



CMOS Inverter Layout



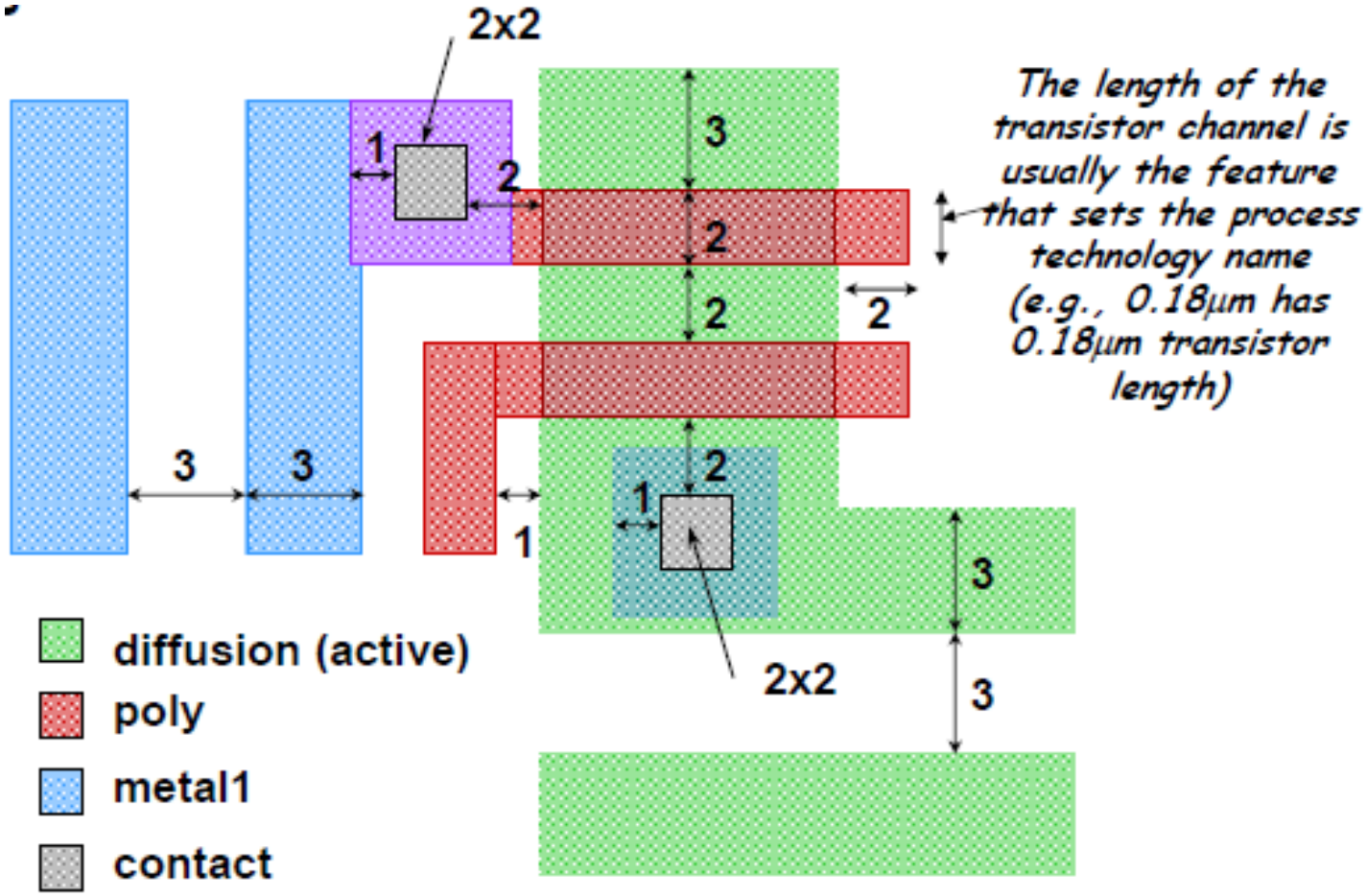
(a) Layout



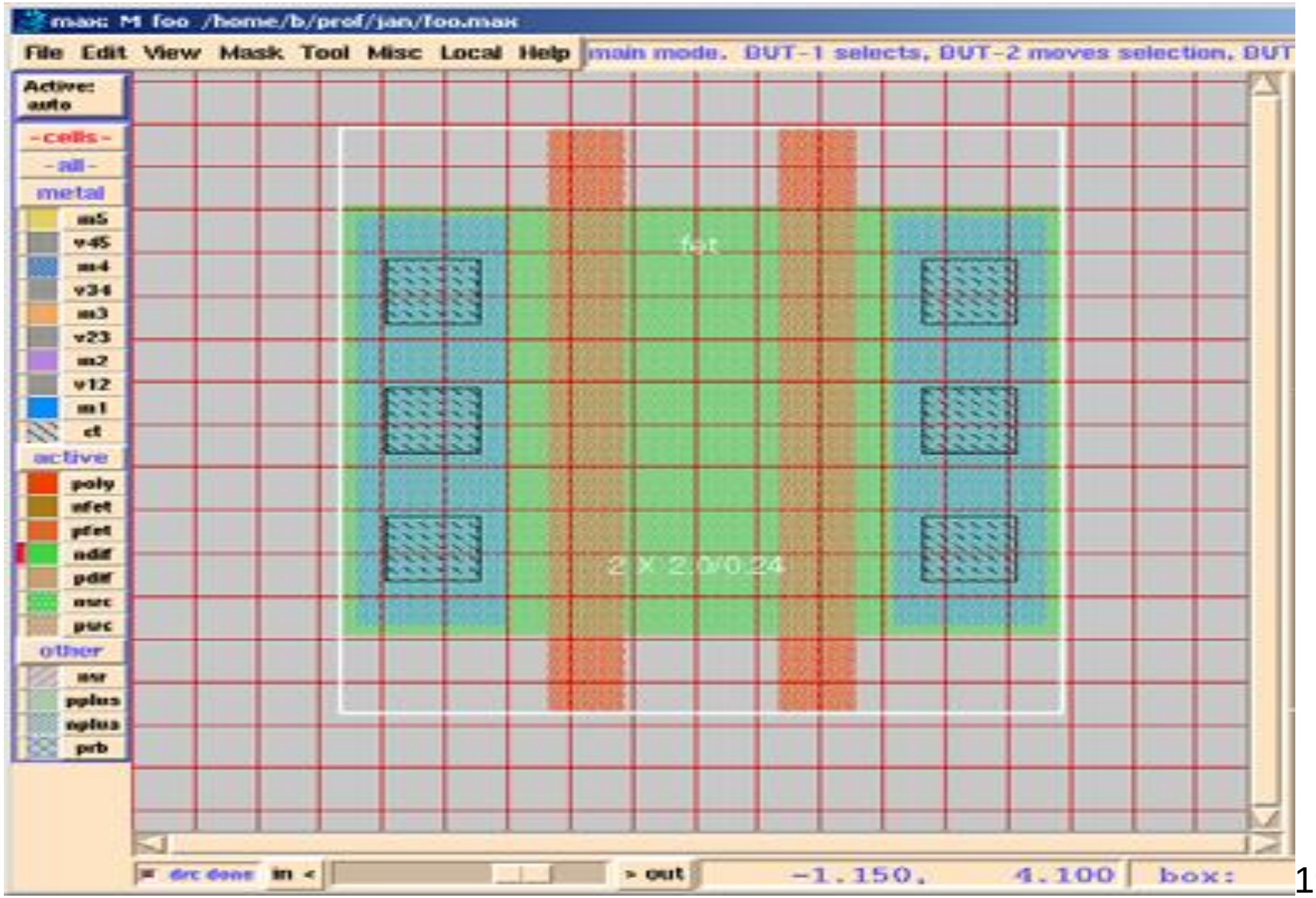
(b) Cross-Section along A-A'

Lambda-based Design Rules

- One lambda (λ)= one half of the "minimum" mask dimension.
- Typically the length of a transistor channel is 2λ.
- Usually all edges must be "on grid", e.g., in the MOSIS scalable rules, all edges must be on a lambda grid.



Layout Editor

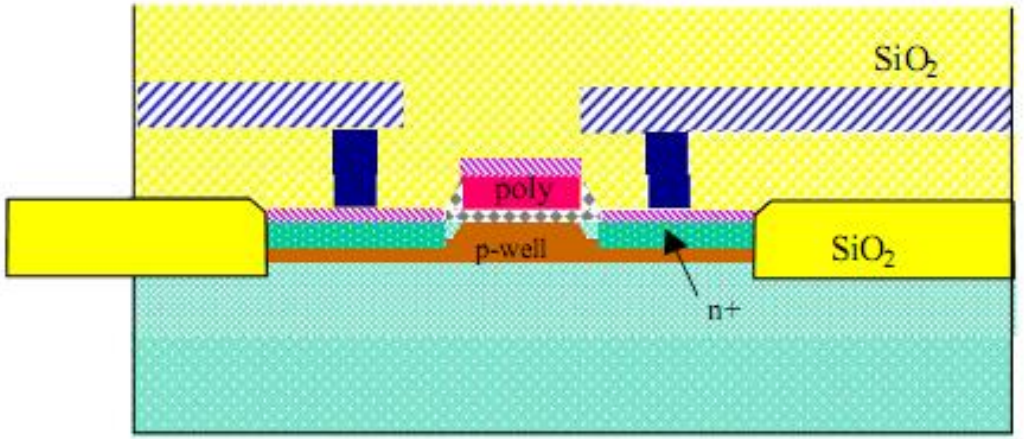


Design Rules

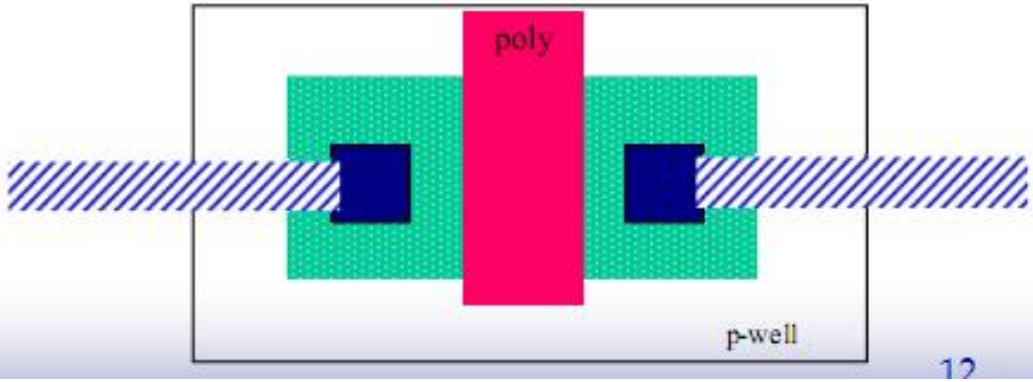
- Intra-layer
  - Widths, spacing, area
- Inter-layer
  - Enclosures, distances, extensions, overlaps
- Special rules (sub-0.25μm)
  - Antenna rules, density rules, (area)

Transistor Layout

Cross-Sectional View



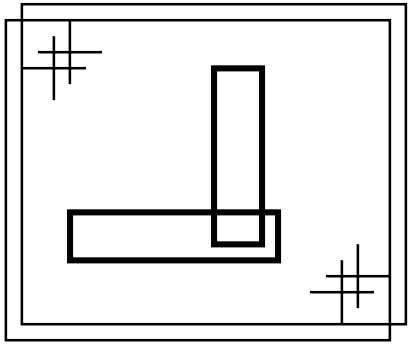
Layout View



Why Have Design Rules?

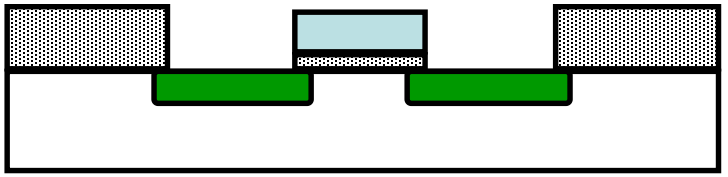
- To be able to tolerate some level of fabrication errors such as

1. Mask misalignment



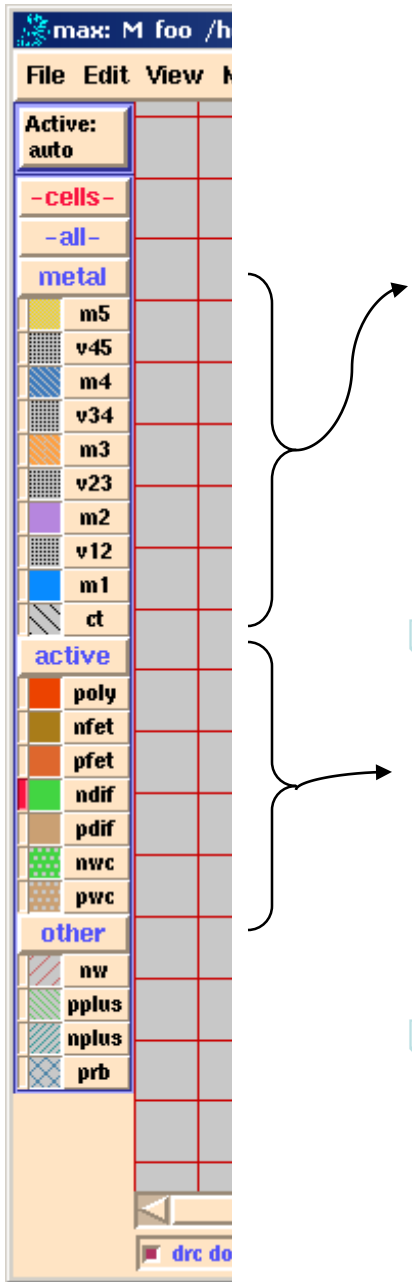
2. Dust

3. Process parameters (e.g., lateral diffusion)



4. Rough surfaces

max Layer Representation

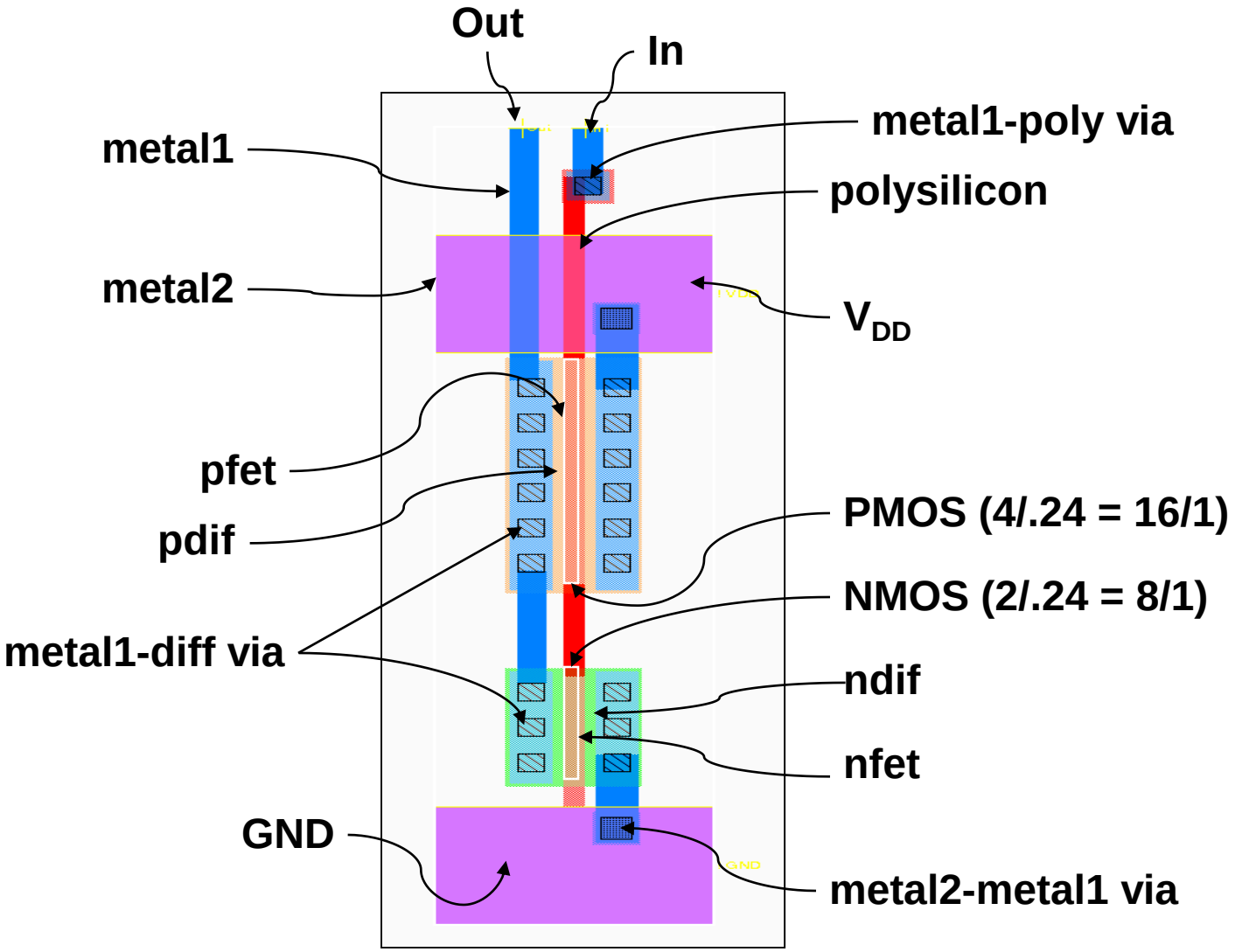


- Metals (five) and vias/contacts between the interconnect levels
  - Note that m5 connects only to m4, m4 only to m3, etc., and m1 only to poly, ndif, and pdif
  - Some technologies support “stacked vias”

- Active – active areas on/in substrate (poly gates, transistor channels (nfet, pfet), source and drain diffusions (ndif, pdif), and well contacts (nwc, pwc))

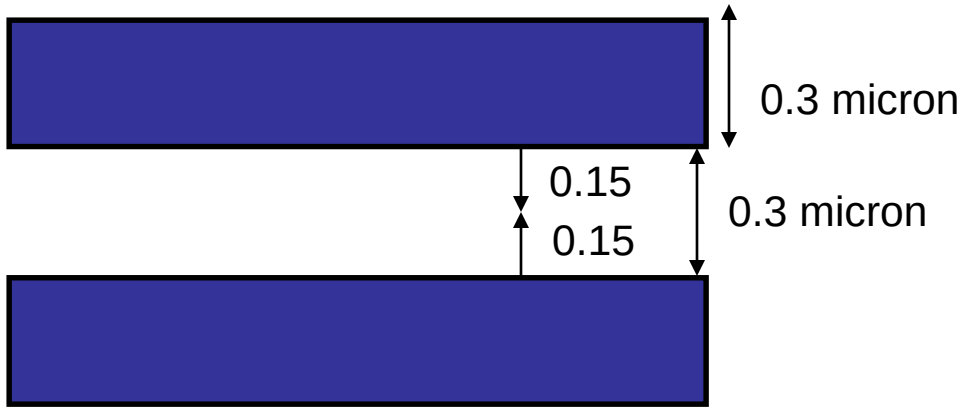
- Wells (nw) and other select areas (pplus, nplus, prb)

CMOS Inverter *max* Layout



Intra-Layer Design Rule Origins

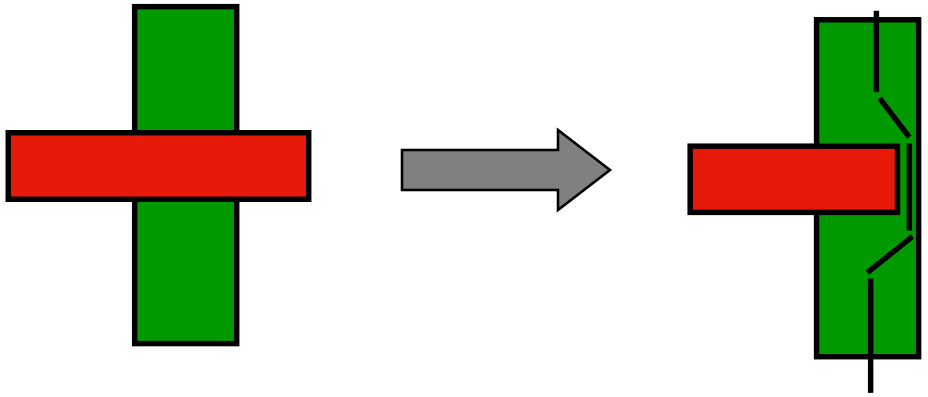
- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
  - minimum line width is set by the resolution of the patterning process (photolithography)
- Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fab



Inter-Layer Design Rule Origins

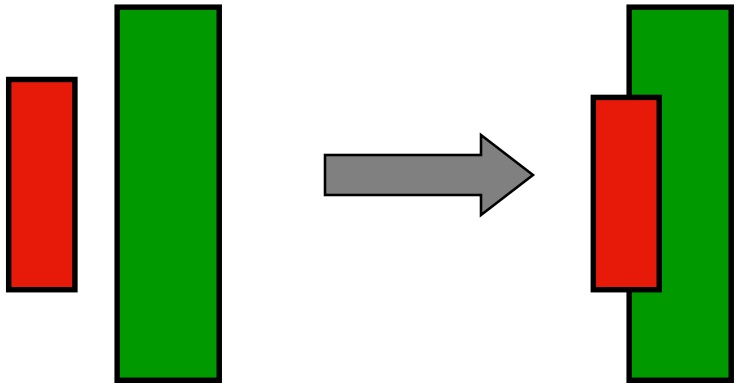
1. Transistor rules – transistor formed by overlap of active and poly layers

Transistors

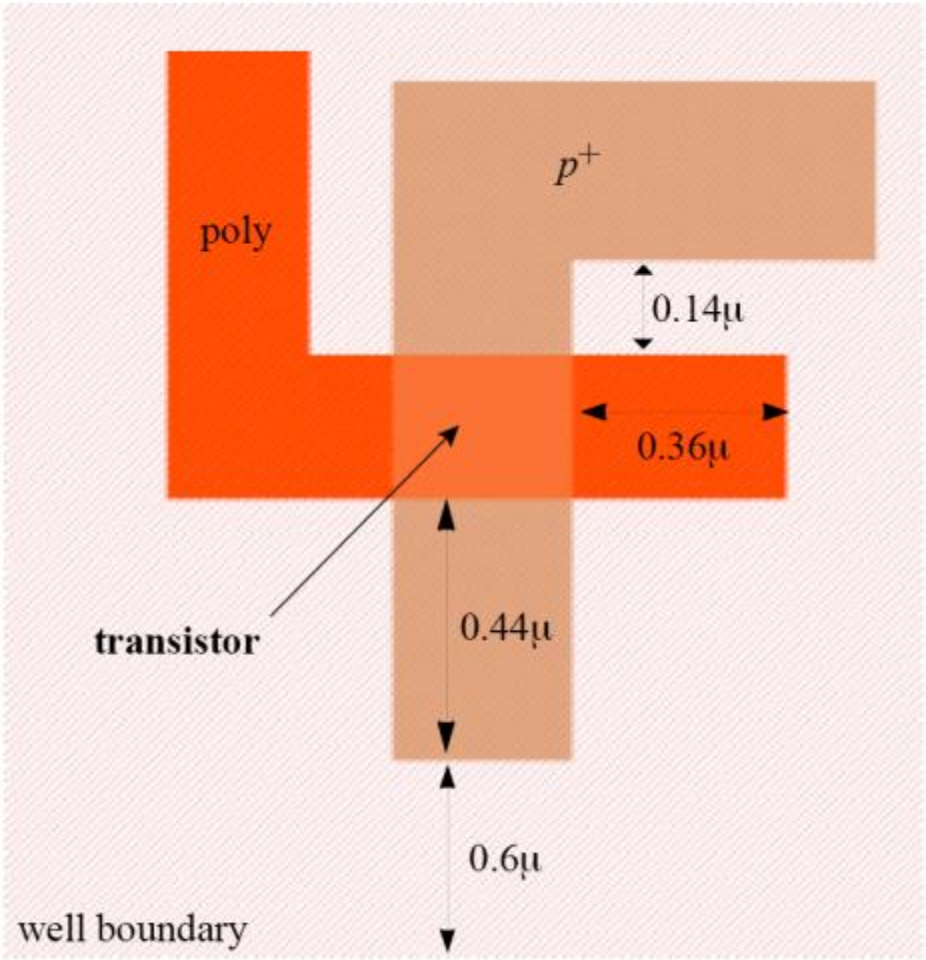


Catastrophic error

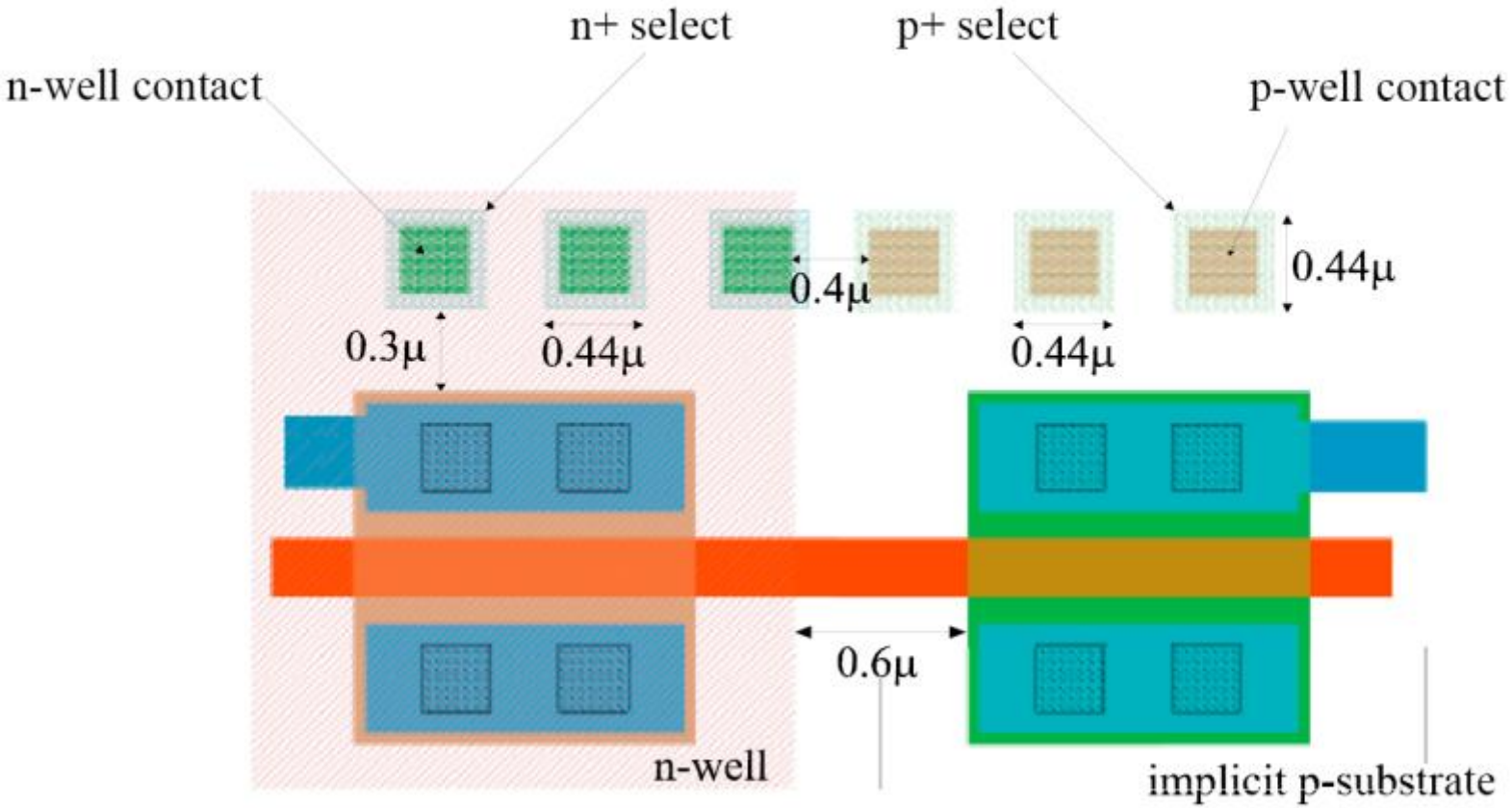
Unrelated Poly & Diffusion



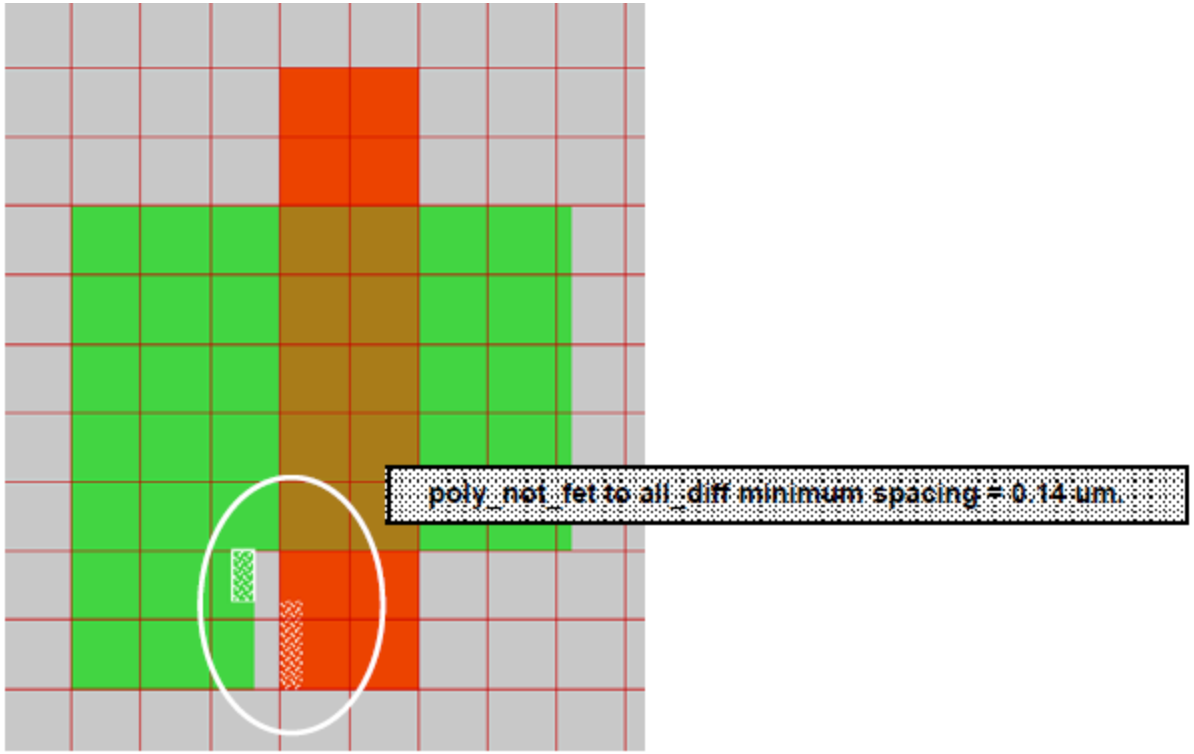
Thinner diffusion, but still working


poly
p^+
0.14μ
0.36μ
transistor
0.44μ
0.6μ
well boundary

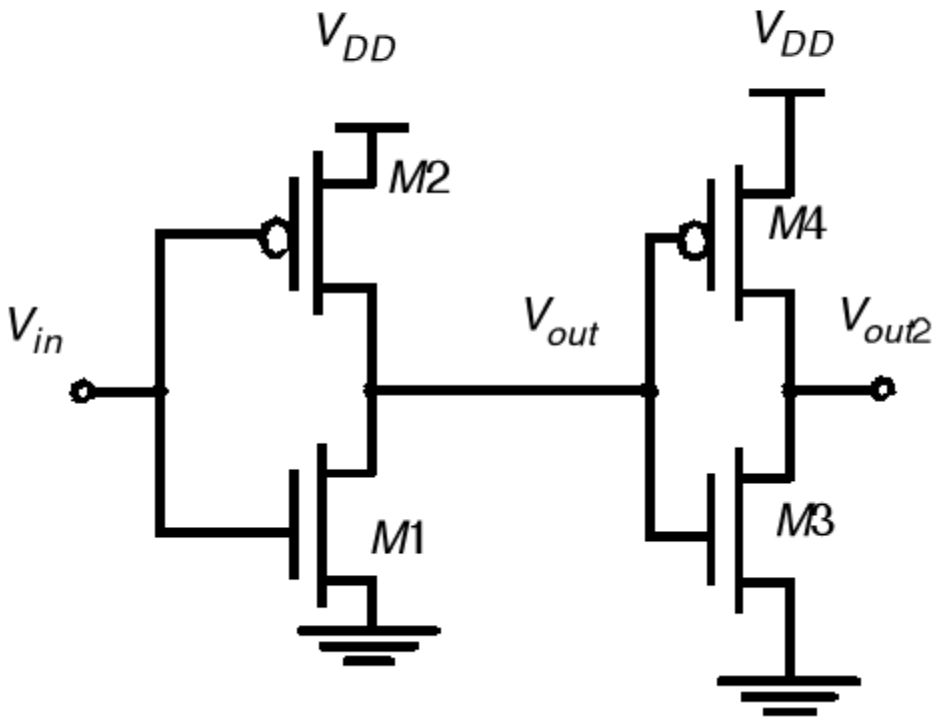
Inter-Layer: Well and Substrate



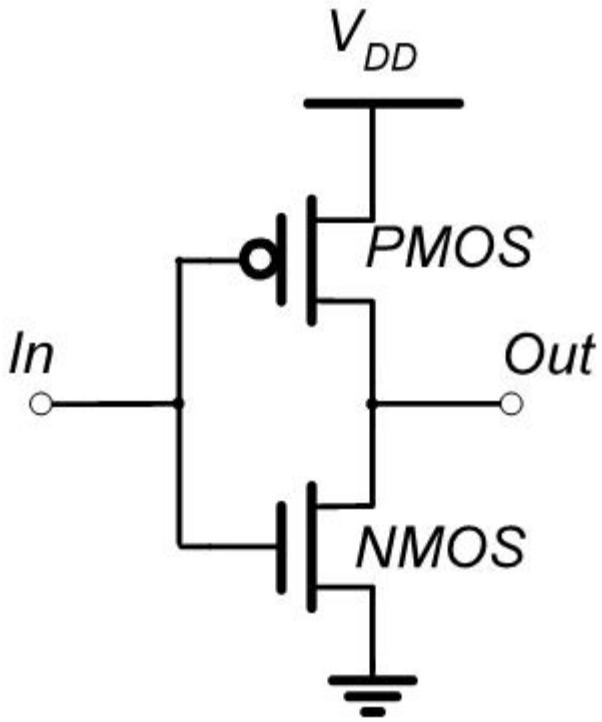
Design Rule Checker

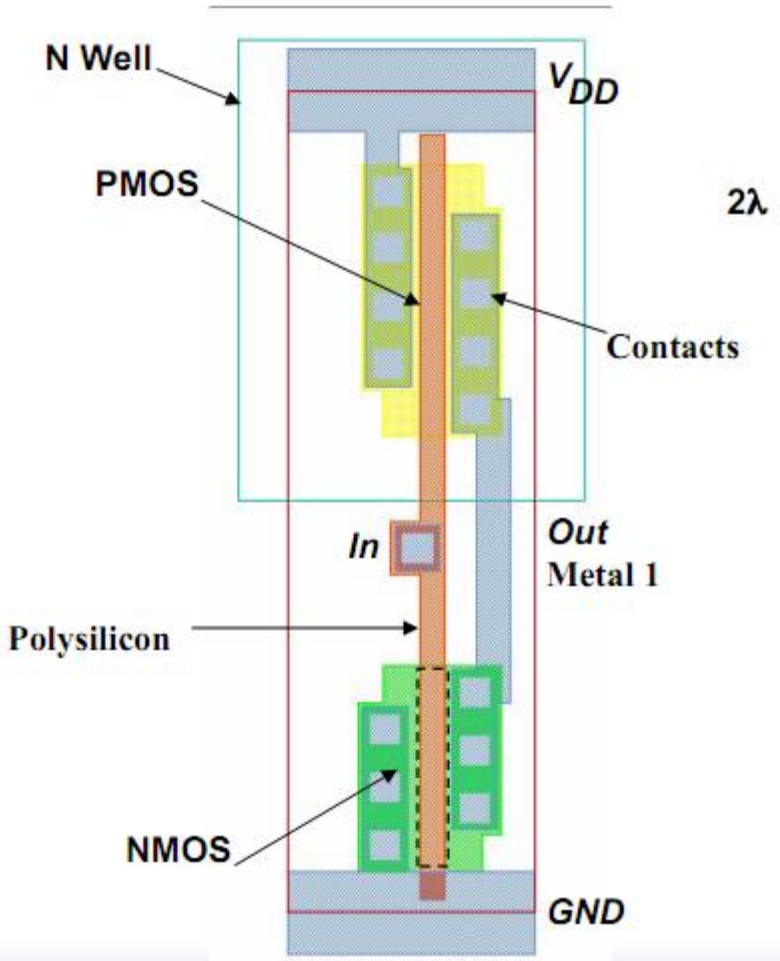


Circuit Under Design



CMOS Inverter

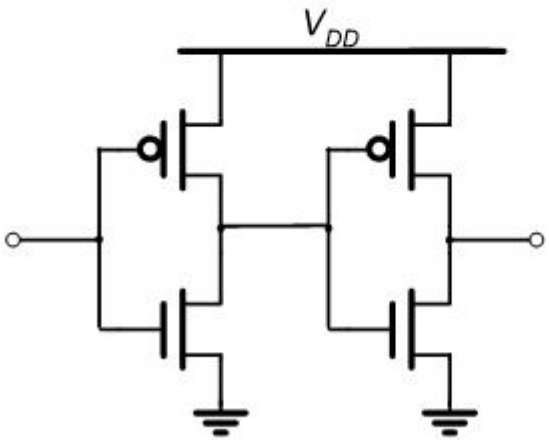


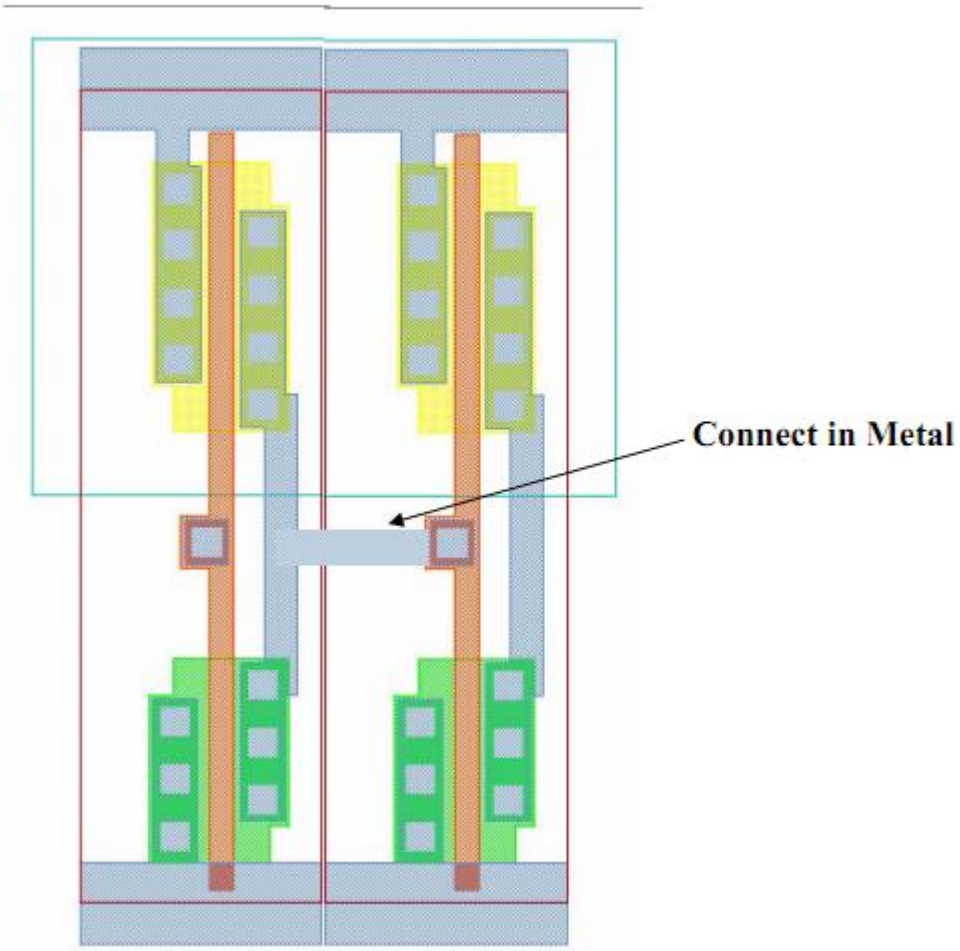


Two Inverters

Share power and ground

Abut cells

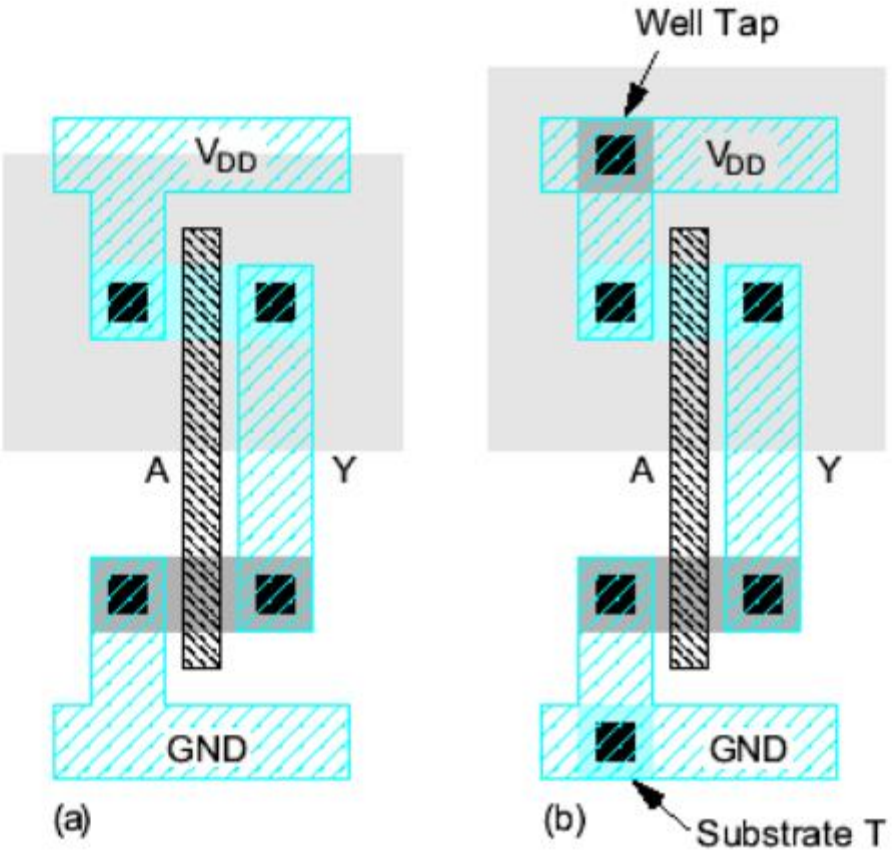




Gate Layout

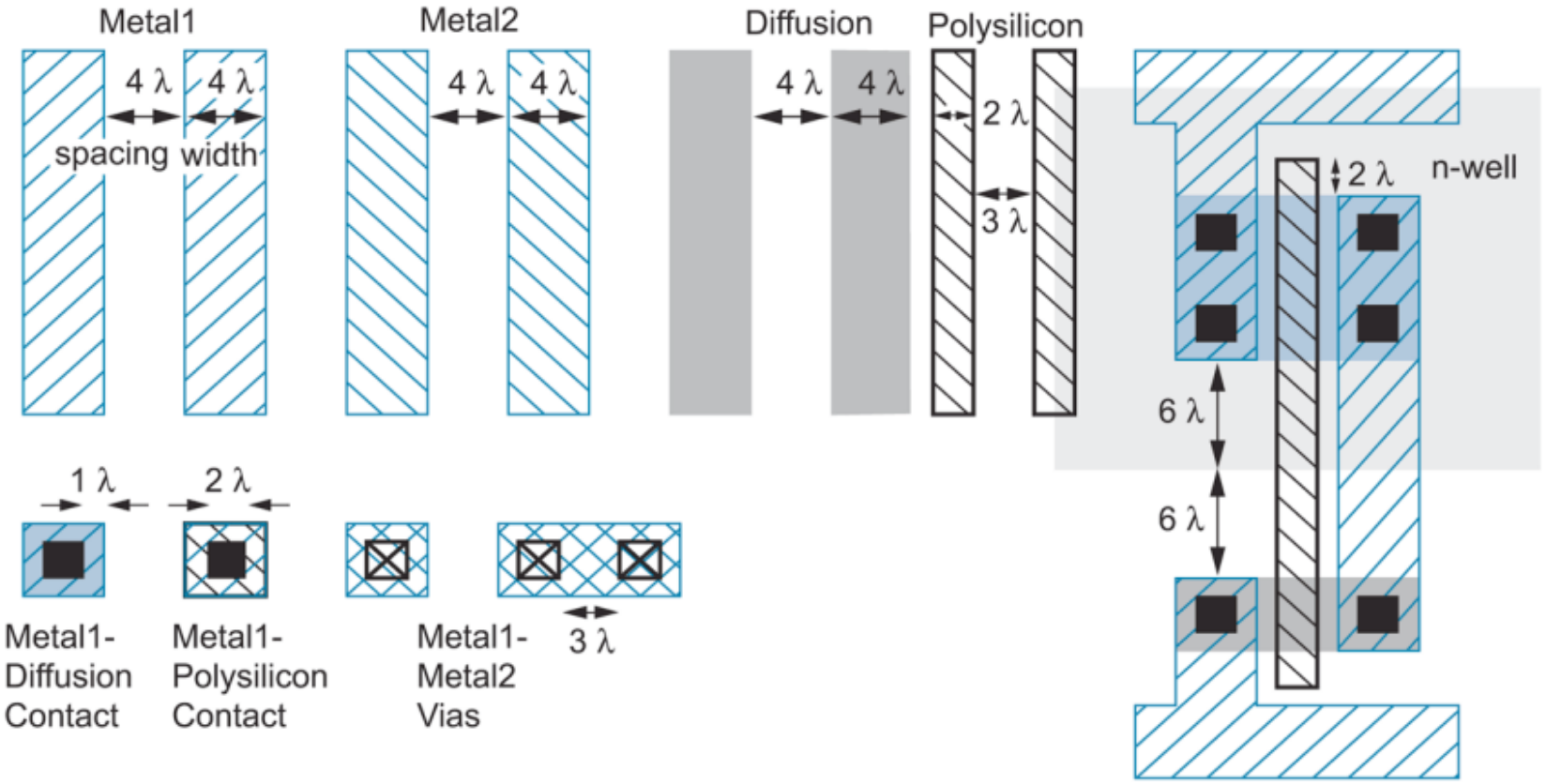
- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - V_{DD} and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts

Example: Inverter



Layout Design Rules

Conservative rules to get started !

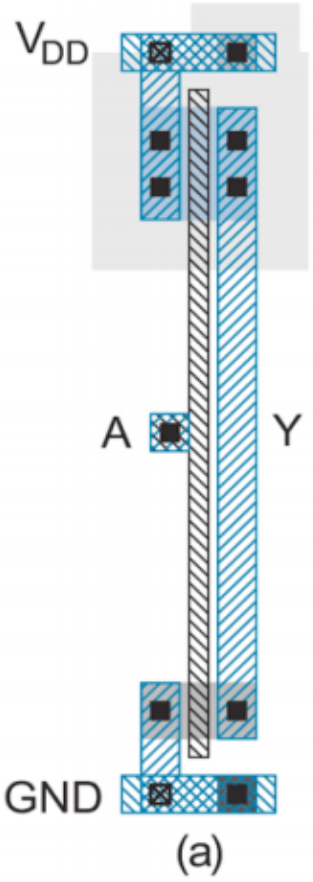


Design Rules Summary

- Metal and diffusion have minimum width and spacing of 4λ
- Contacts are 2λ x 2λ and must be surrounded by 1λ on the layers above and below
- Polysilicon uses a width of 2λ
- Polysilicon overlaps diffusions by 2λ where a transistor is desired and has spacing or 1λ away where no transistor is desired
- Polysilicon and contacts have a spacing of 3λ from other polysilicon or contacts
- N-well surrounds pMOS transistors by 6λ and avoid nMOS transistors by 6λ

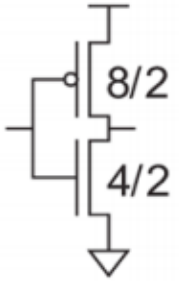
The power and ground lines are called supply rails

Inverter Layout

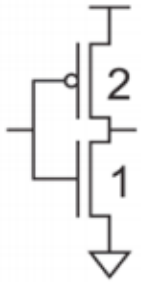


(a)

- Transistor dimensions specified as W / L ratio
- Minimum size is 4λ / 2λ, sometimes called 1 unit



(b)



(c)

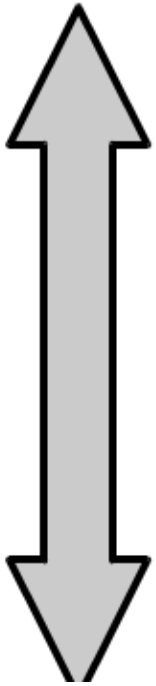
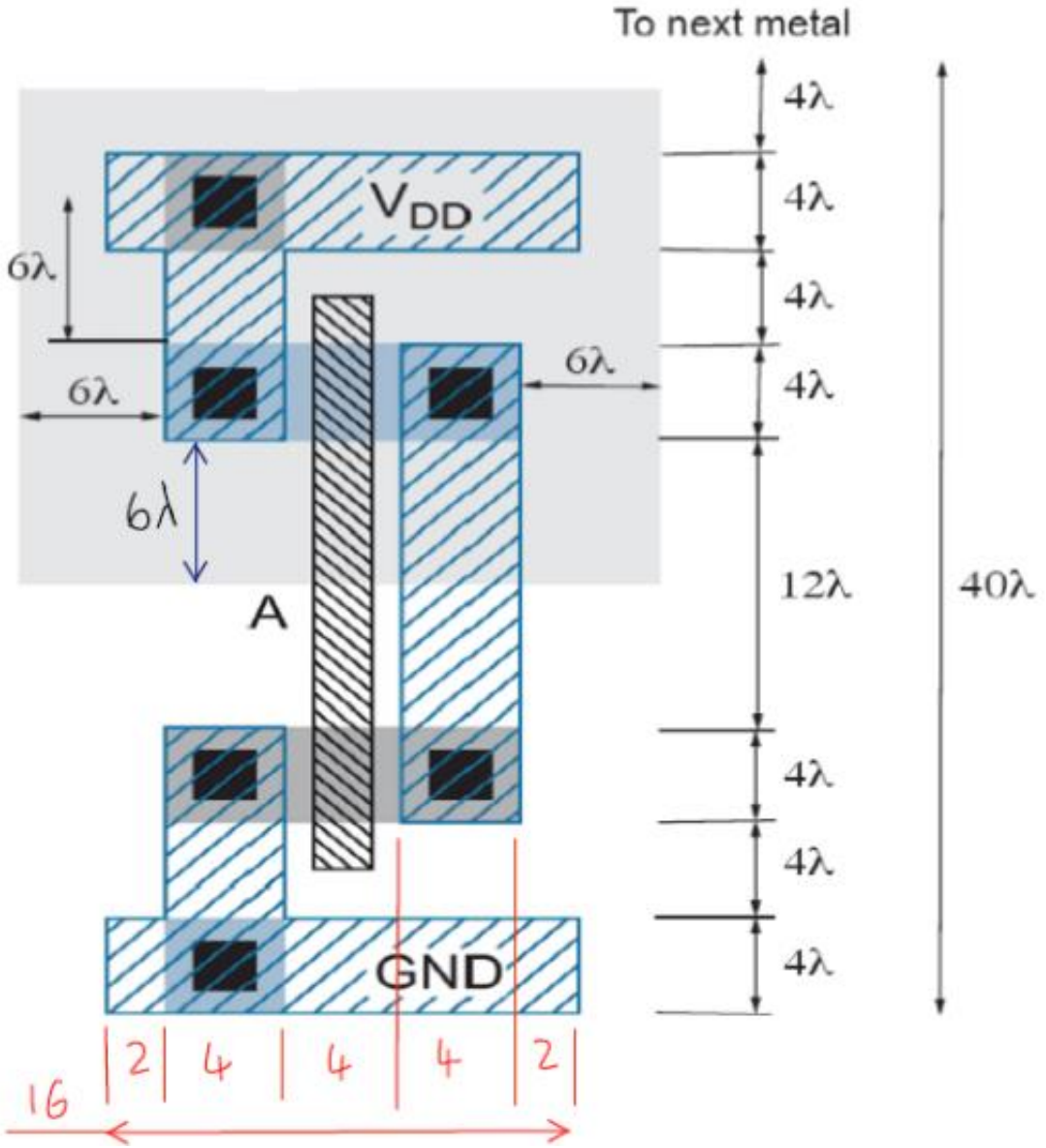
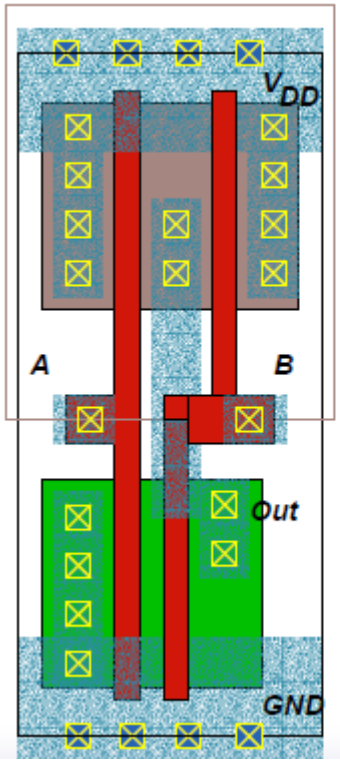


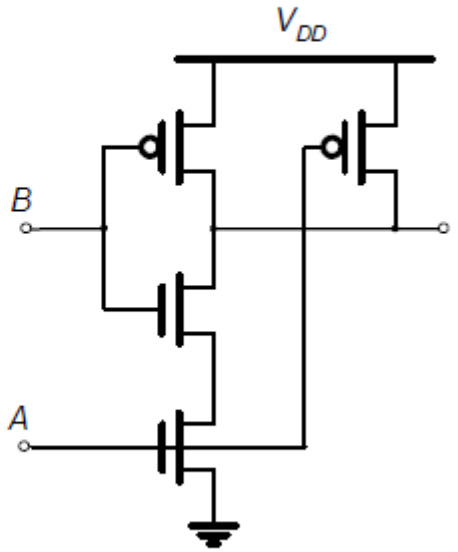
FIG 1.40 Inverter with dimensions labeled

Inverter Standard Cell Area (1/2

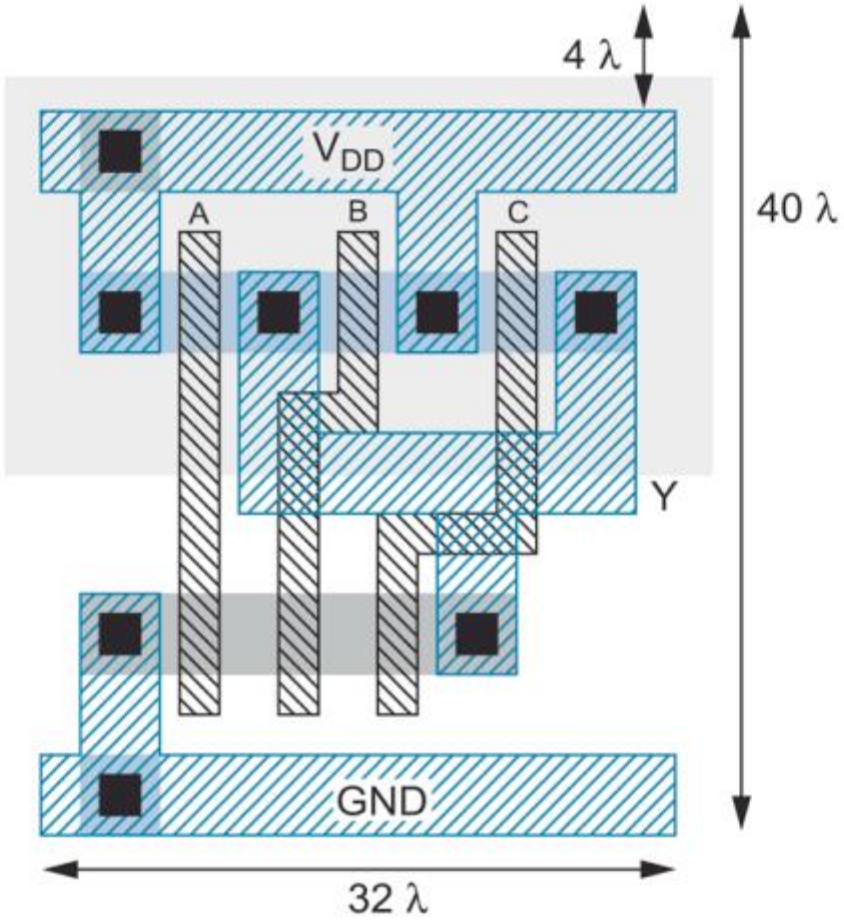




2-input NAND gate

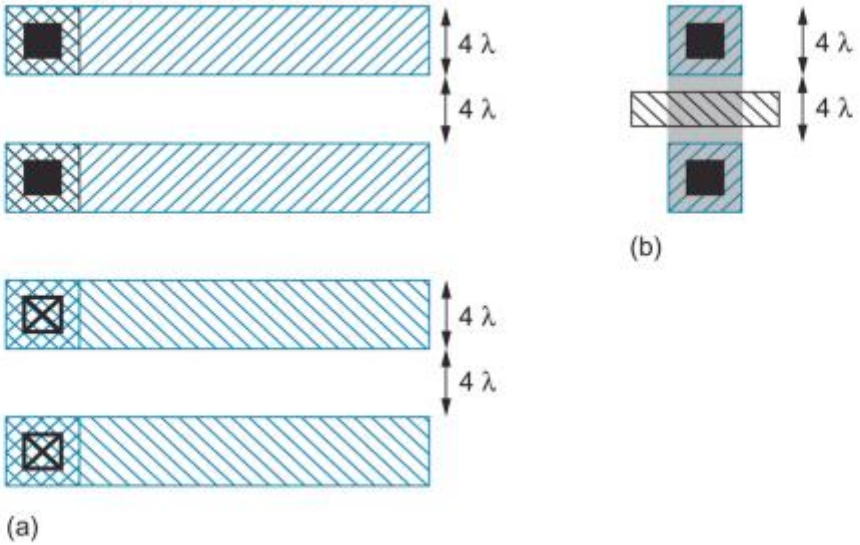


3-input Standard Cell NAND



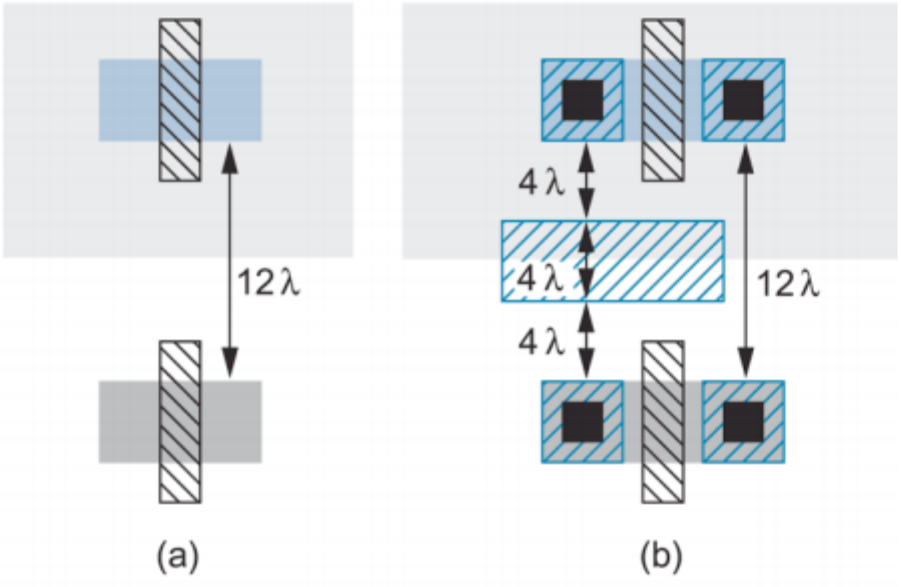
Wiring Tracks

- A **wiring track** is the space required for a wire
  - 4λ width, 4λ spacing from neighbor = 8λ pitch
  - Transistors also consume one wiring track



Well Spacing

- Wells must surround transistors by 6λ
  - Implies 12λ between opposite transistor flavors
  - Leaves room for one wire track

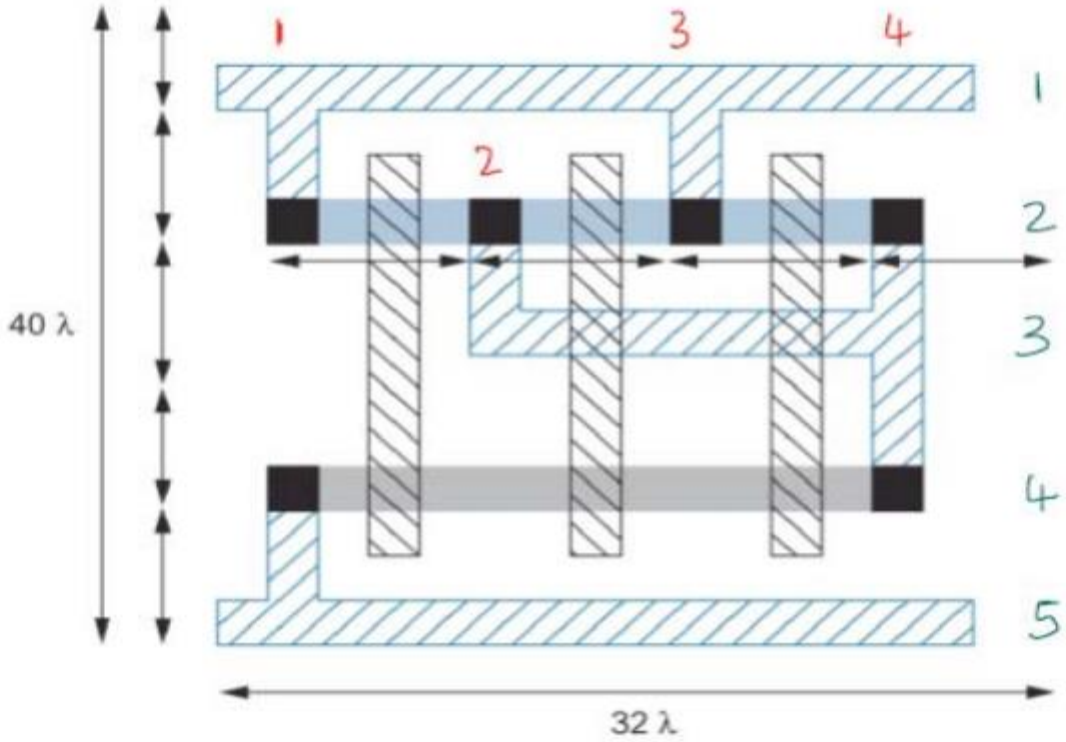


Area Estimation

- Estimate area by counting wiring tracks
  - Multiply by 8 to express in λ

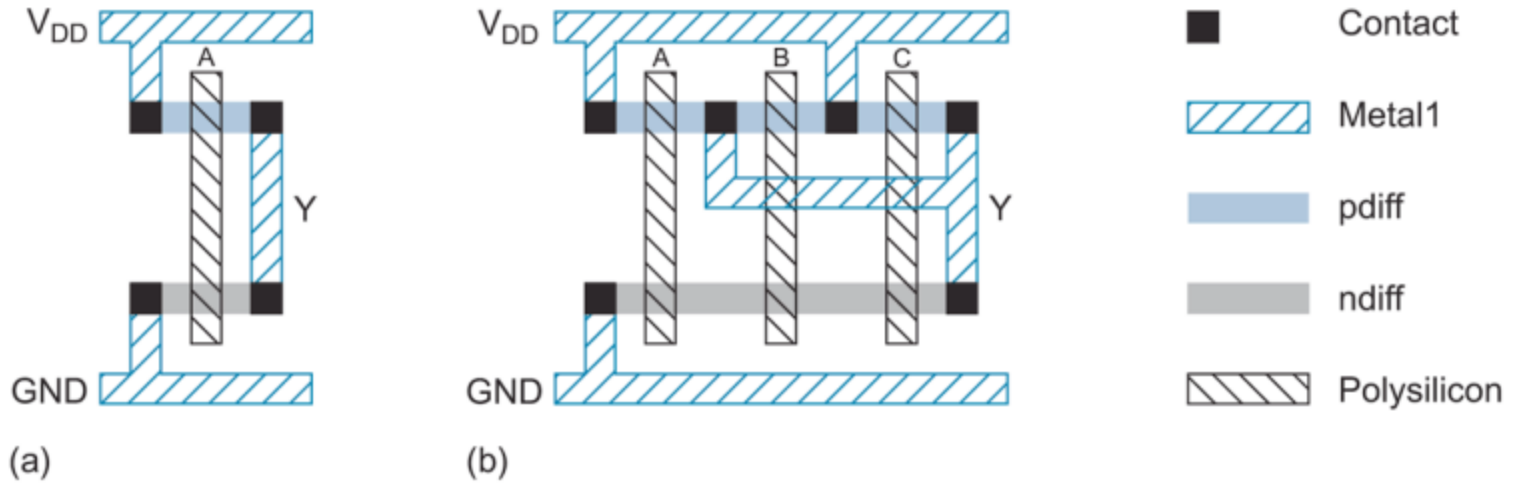
Horizontal
4 × 8 = 32

Vertical
5 × 8 = 40



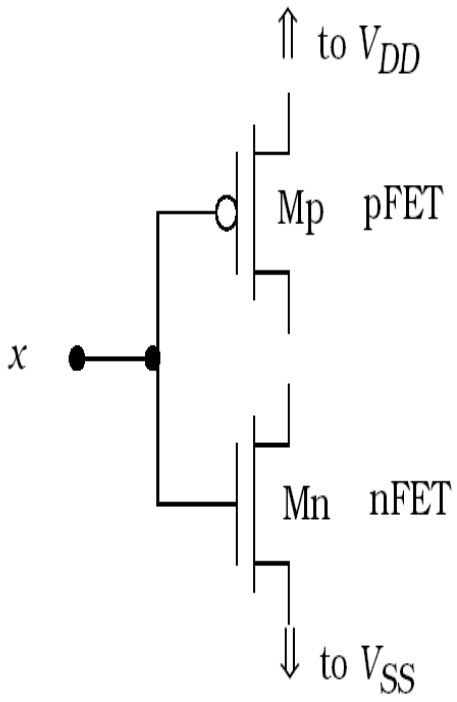
Stick Diagrams

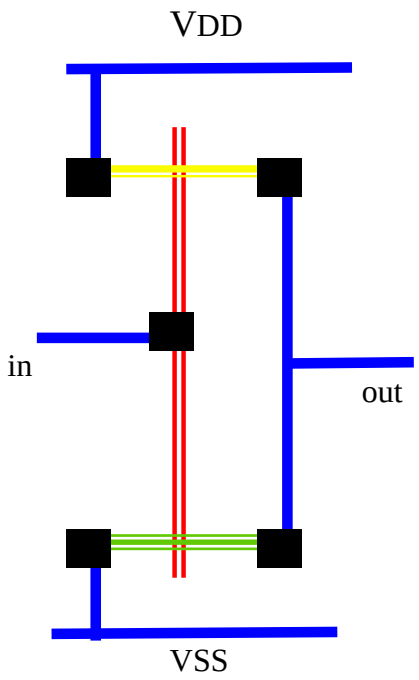
- **Stick diagrams** help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers

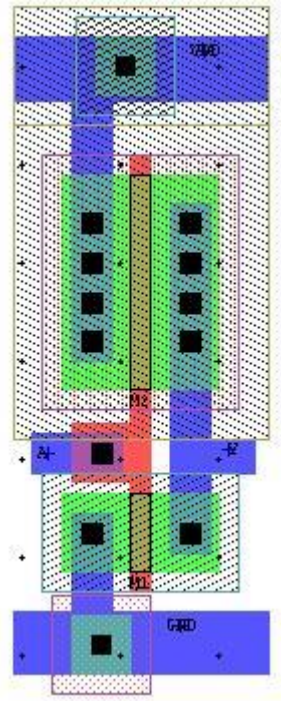


CMOS Inverter Stick Diagrams

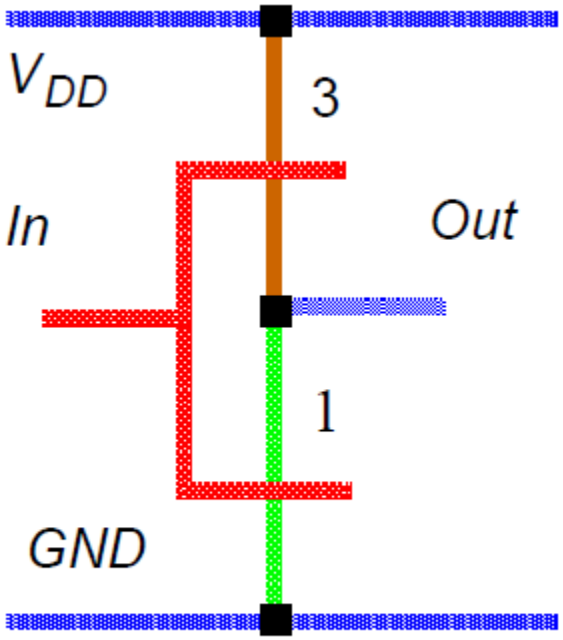
- **CMOS inverter described in other way.**







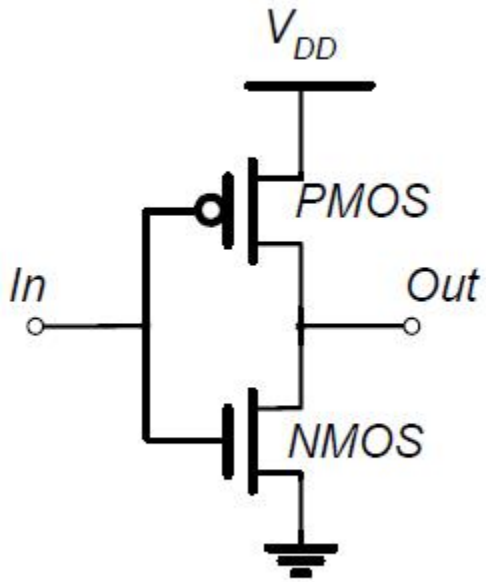
Sticks Diagram

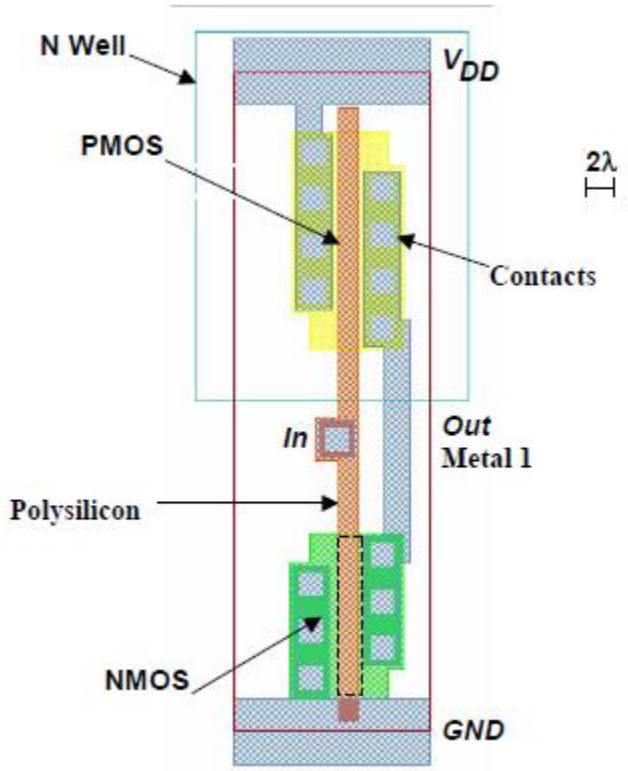


Stick diagram of inverter

- Dimensionless layout entities
- Only topology is important
- Final layout generated by "compaction" program

CMOS Inverter

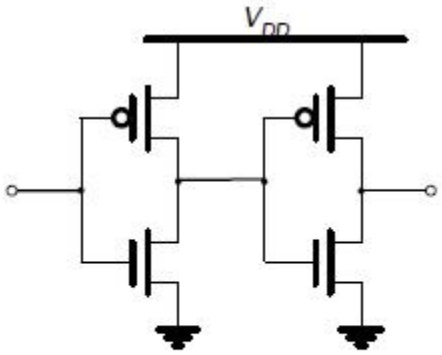


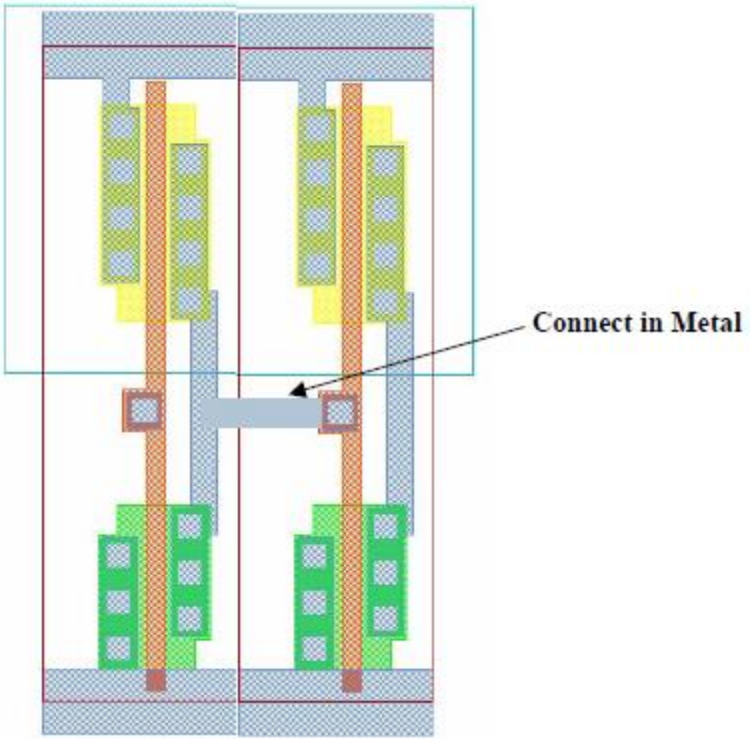


Two Inverters

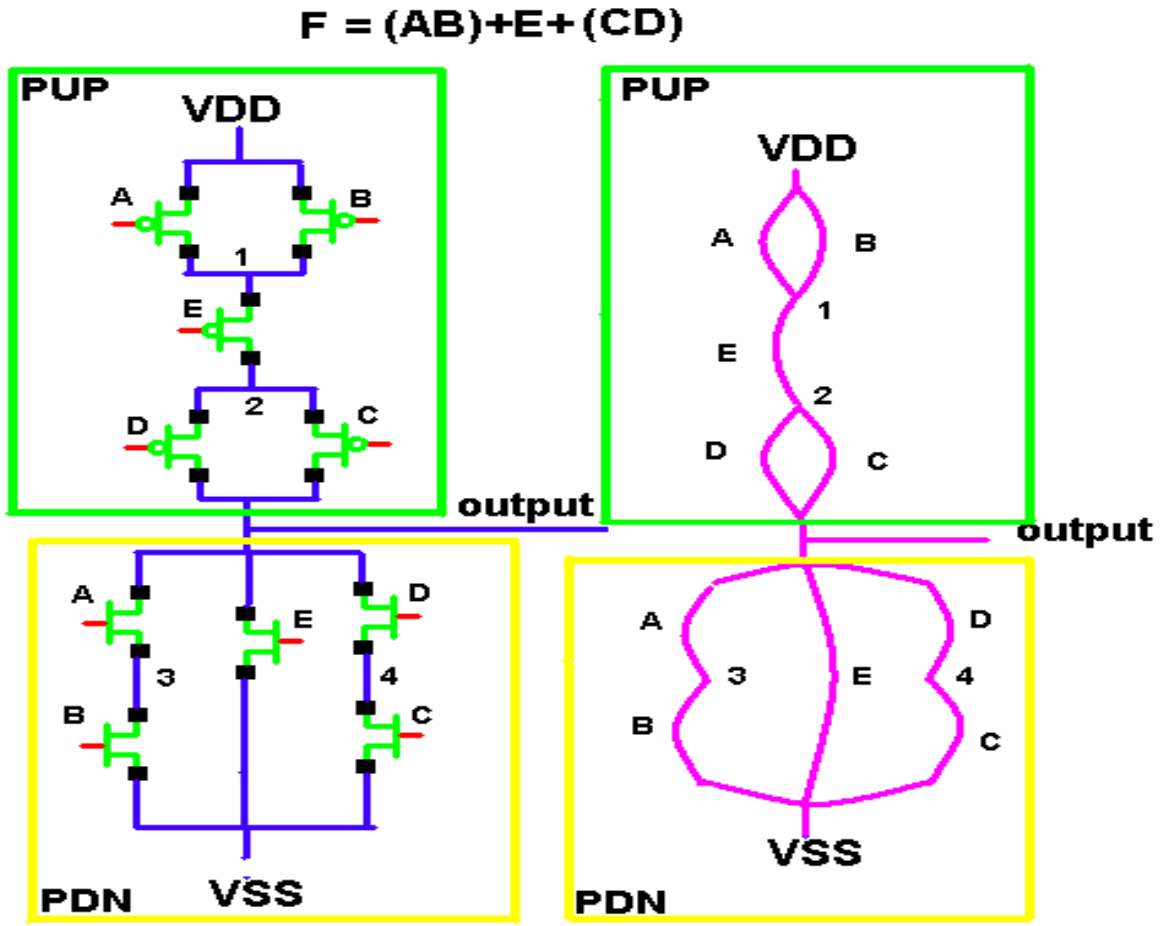
Share power and ground

Abut cells





Stick Diagram

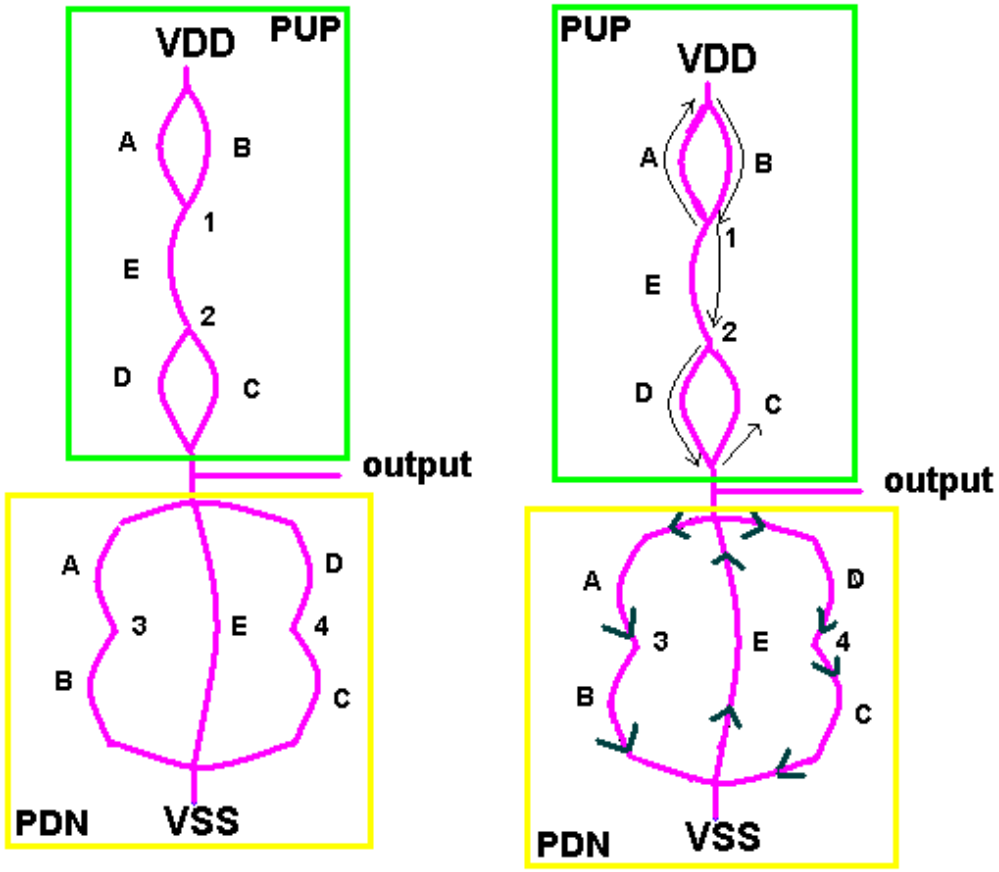


Identify each transistor and connection to the transistor by a unique name

construct a logic graph

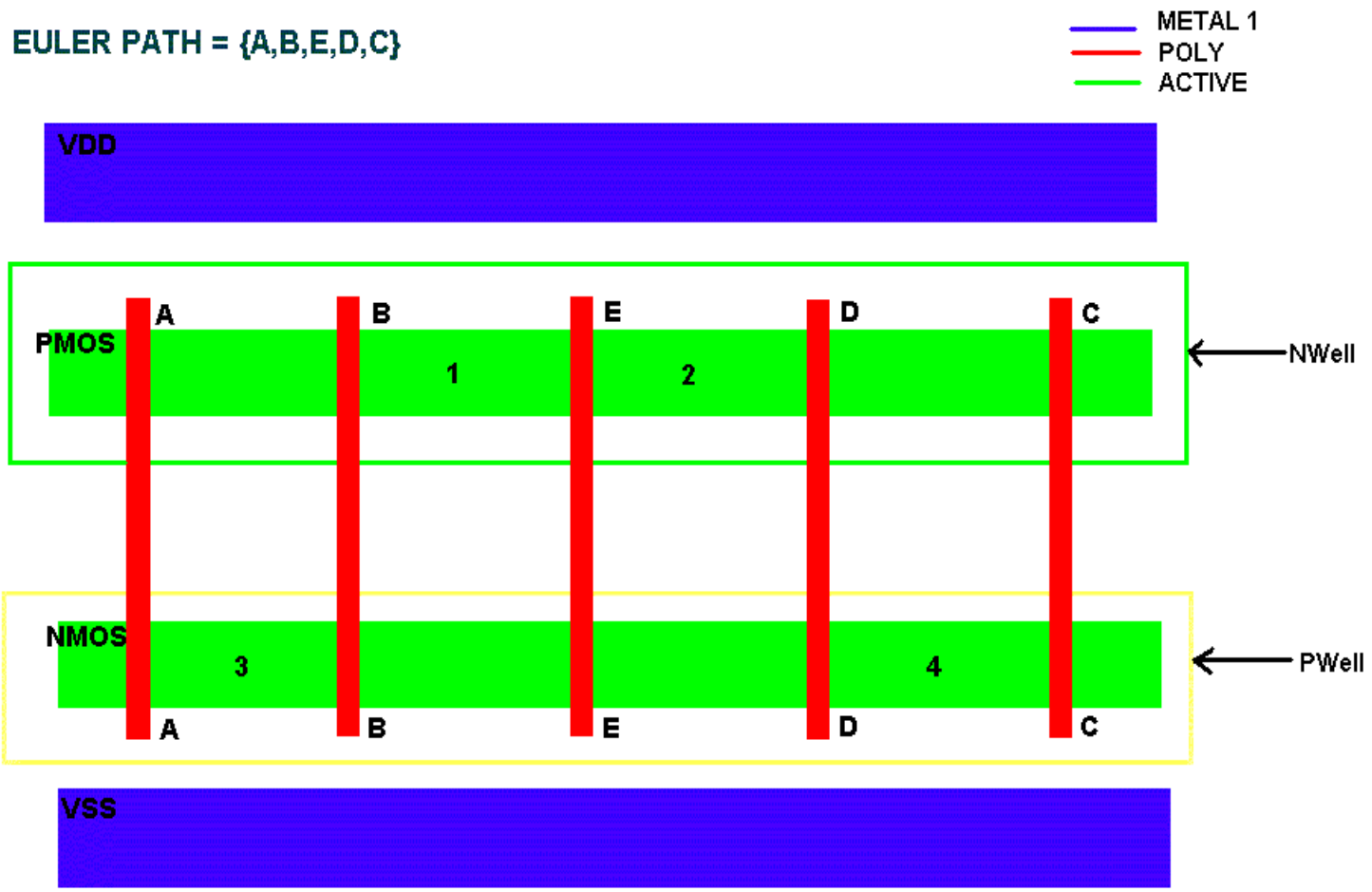
F = (AB)+E+(CD)

See the tutorial for further details.



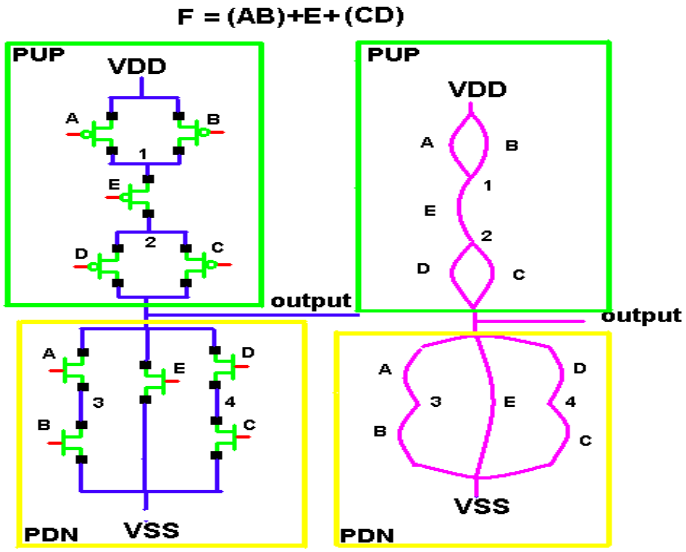
EULER PATH = {A,B,E,D,C}

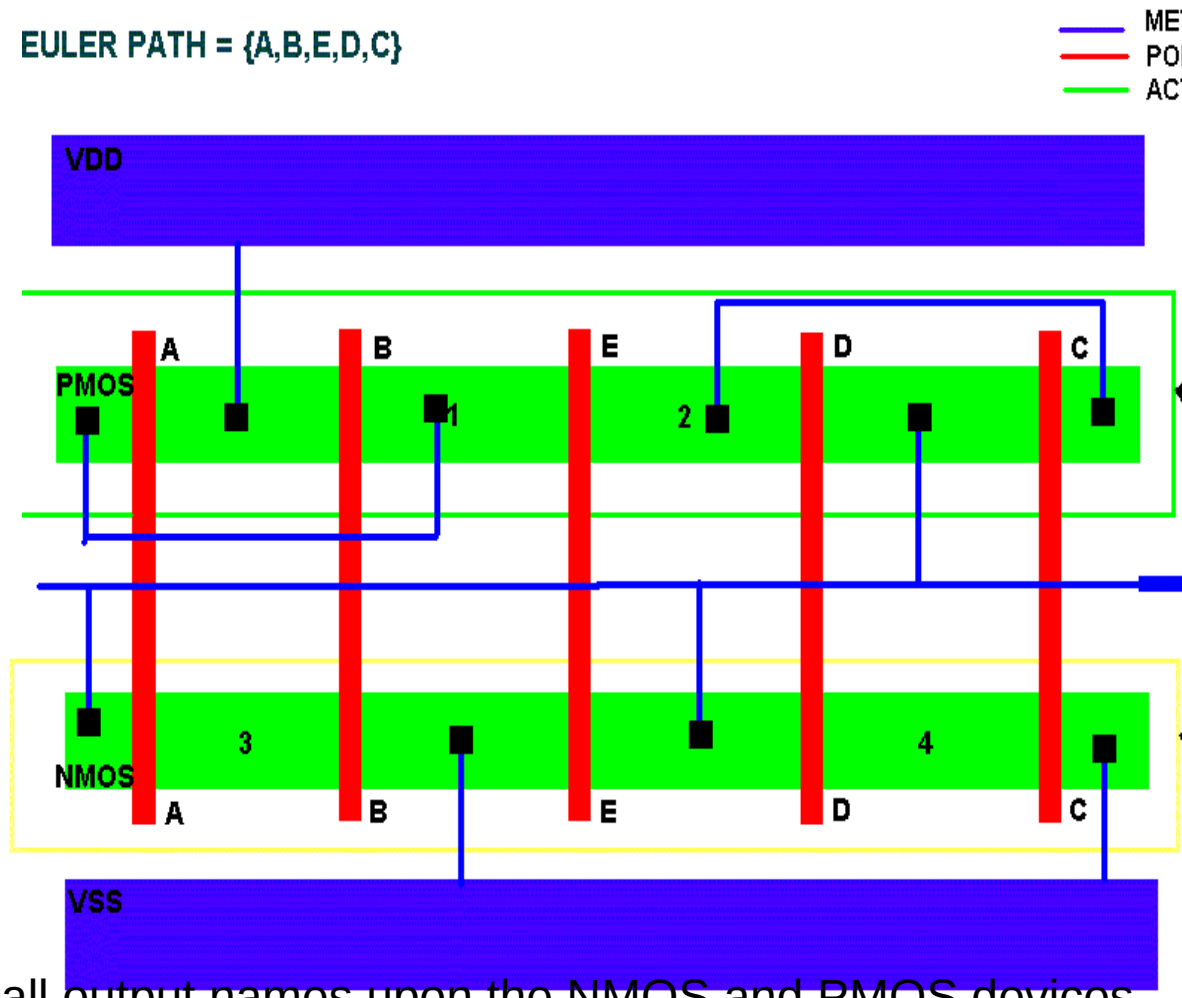
- construct one Euler path for both the Pull up and Pull down network



-Trace two green lines horizontally to represent the NMOS and PMOS devices and surround them by n and p-wells
-Trace the number of inputs (5 in this example) vertically across each green strip and label them in order.
-Trace blue lines to represent VDD and VSS
-Place the connection labels upon the NMOS and PMOS devices

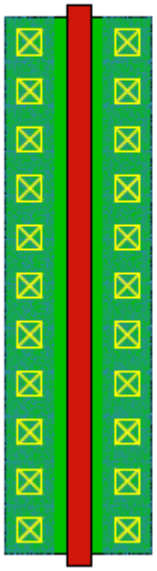
.



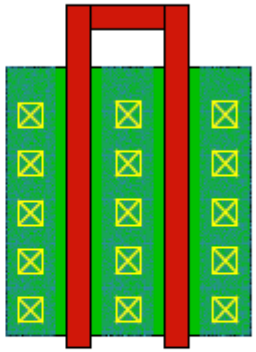


-Place the VDD, VSS and all output names upon the NMOS and PMOS devices
-interconnect the devices based on Euler path.

One finger

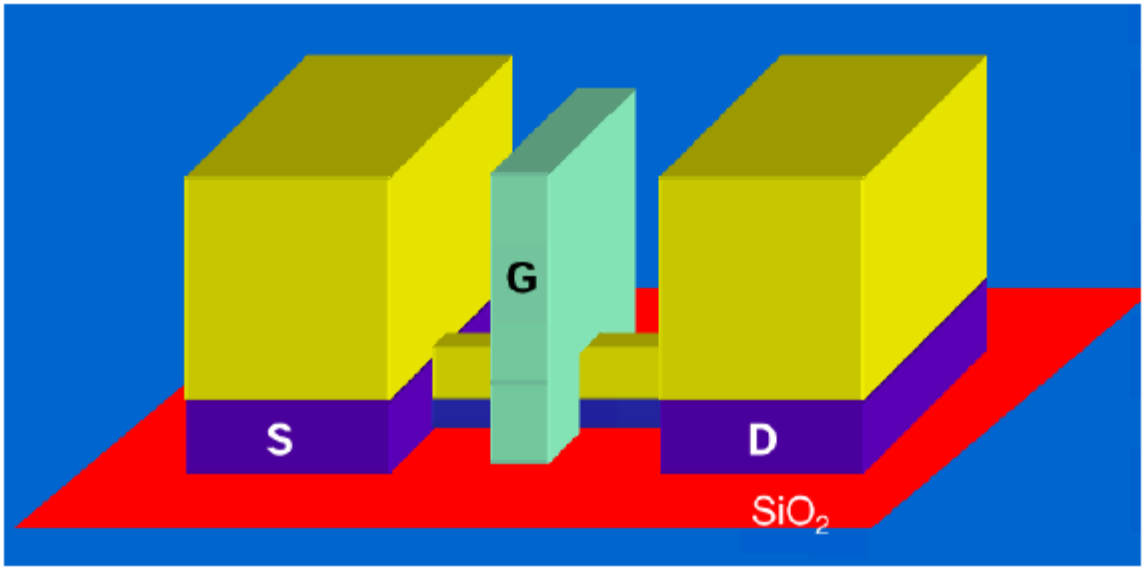


Two fingers (folded)



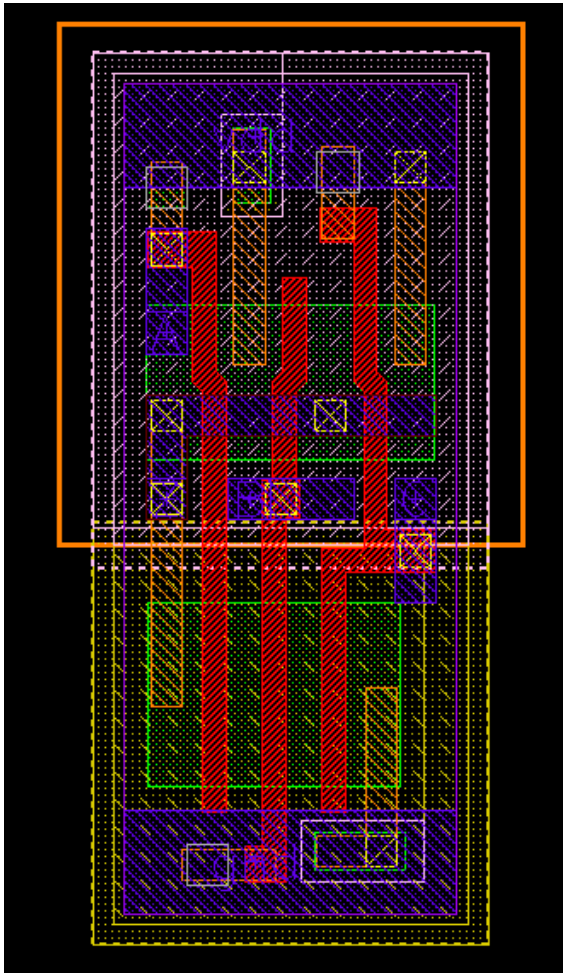
Less diffusion capacitance

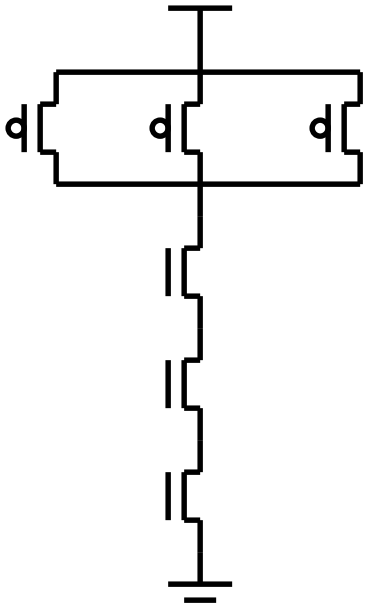
Future device



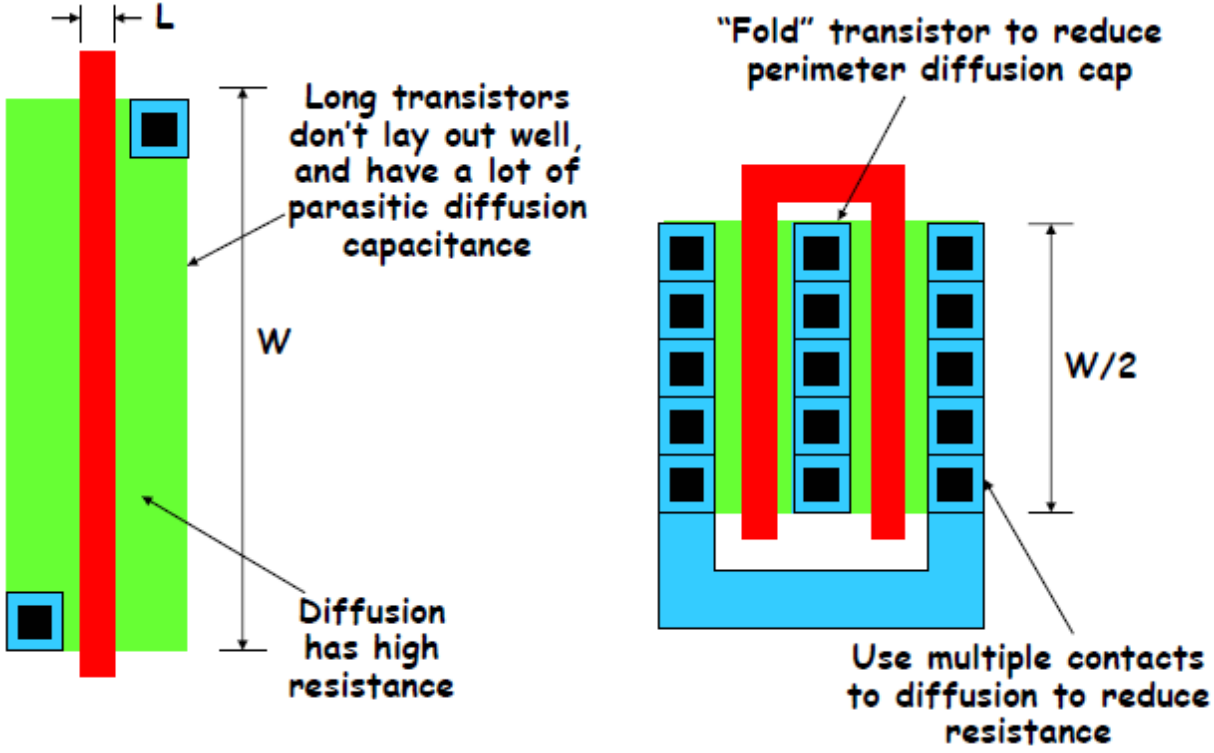
25 nm MOS transistor (Folded Channel)

Layout vs. Schematic





Gate Layout Tricks



Gate Layout Tricks